A System on Chip (SOC) – Highperformance Power Drive Applications - SVPWM based Voltage Source Inverter

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ABSTRACT

This paper presents a new circuit realization on single on chip for the space-vector pulse-width modulation (SVPWM) strategy. An SVPWM control integrated circuit (IC) has been developed using the state-of-the-art field-programmable gate array (FPGA) technology. The proposed SVPWM control scheme can be realized using only a single FPGA (XC4010) from Xilinx, Inc. presents the design and Implementation of library modules called Intellectual Property (IP) Cores to develop high-performance power drives and motion control applications. The Library is coded in VHDL for modularity and portability. Very frequently Power Drives and motion control applications are implemented using DSP or Microcontroller and algorithms are written in assembly or in a high level language such as 'C.' By using VHDL to describe the circuit we implement algorithms directly in hardware instead of writing sequential programs. The realization includes the module of the implementation of Space Vector Pulse Width Modulation (SVPWM) switching patterns for three phases Voltage Source Inverters (VSI) which plays a vital role in the induction machine control. The objectives is to present a survey on the advancement recently introduced in the design of electronic circuits and to discuss how they can be implemented in Industrial Electronics industry to pace with the new wave of global competition. In this work a methodology for developing the IP cores for Power Drive and Motion Control Applications is proposed. The advantages of this implementation are to reduce the cost by embedding them in a single chip, to achieve the processing speed incomparable to that of sequential flow program of DSP's and Microprocessors, to make them application specific and they can be enhanced to suit future complex requirements.

1. INTRODUCTION

The Pulse Width Modulation (PWM) Technique called "Vector Modulation", which is based on space vector theory, is the most important development in the last few years [2]. Although, several of PWM methods have been created in the past, the vector modulation technique appears to be the best alternative for a three phase switching power converter [1], [4]. It provides an optimization of converter Operation, reducing the commutations of the power semiconductor. There are some previous implementations of this technique which had shortcomings. Firstly [2], discrete components, principally ROM and counter, are combined together. Switching times are calculated and then stored in ROM, resulting in a simple circuit. However, the frequency of motor speed is difficult to control and the system is not compact. Secondly, a fast microprocessor is employed to calculate some parameters. However, to obtain higher switching frequency, a fast processor, such a DSP [3], [6], is
necessary resulting in high cost, and also, a long time is required to develop software in a new processor structure. Moreover, processor controlled by software is not suitable for a switching power circuit, which generates a lot of noise, resulting in High-risk of collapse. This paper presents a different and better solution for the practical implementation of the modulator, achieving many advantages. The design used Xilinx development tools, namely Work view, and is realized in a single
FPGA chip with no external memory. The benefits of this design are as follows: ·

- The whole system is implemented in only a single chip consequently the circuit is very compact.
- Systems on a FPGA chip are more reliable because they do not need any Control software.
- Faster design and verification time, design change without penalty [7].

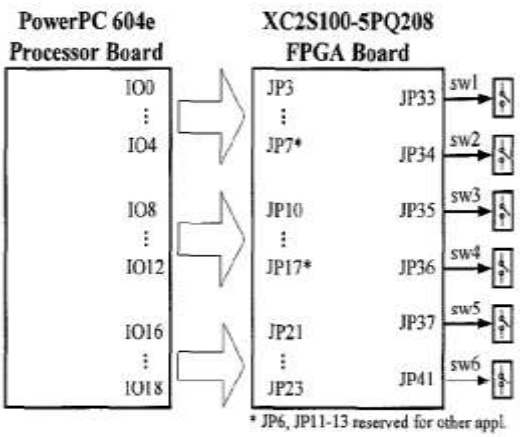


Fig 1.Circuit schematics of the designed PWM pattern generator

I. REVIEW OF SVPWM THEORY

Space Vector PWM refers to a special switching scheme of the six power transistors of a three phase power converter. It generates minimum harmonic distortion to the currents in the windings of a 3 phase AC motor. It also provides more efficient use of supply voltage in comparison with the sinusoidal modulation method [5]. There are eight possible combinations of switching patterns for the three upper switches of the inverter shown in Fig.1.

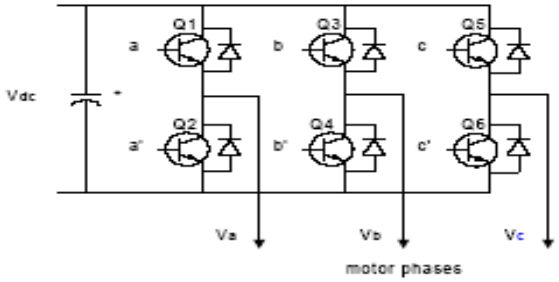


Fig.1.Three phase power inverter diagram

TABLE I

INVERTER SWITCHING STATES

a	b	c	V_a	V_b	V_c	V_{ab}	V_{bc}	V_{ca}
0	0	0	0	0	0	0	0	0
1	0	0	2/3	-1/3	-1/3	1	0	-1
1	1	0	1/3	1/3	-2/3	0	1	-1
0	1	0	-1/3	2/3	-1/3	-1	1	0
0	1	1	-2/3	1/3	1/3	-1	0	1
0	0	1	-1/3	-1/3	2/3	0	-1	1
1	0	1	1/3	-2/3	1/3	1	-1	0
1	1	1	0	0	0	0	0	0

The phase and line to line voltages generated by each of these combinations can be calculated from (1) and are

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1)$$

Expressed as a fraction of inverter input voltage Vdc. The results of this are presented in Table. I. For each switching combination a voltage space vector can be constructed using (2).

$$V^* = \frac{2}{3}(v_a + a v_b + a^2 v_c) \quad (2)$$

When these space vectors are plotted on a set of real and imaginary axes the switching diagram in Fig.2. is obtained. The switching space vectors divide the axes into 6 equally sized sectors. The two null vectors V7(000) and V8(111) are located at the origin. The objective of SVPWM is to approximate a reference space vector V* somewhere within the transcribed circle of Fig.2 using a combination of the eight switching vectors. One method is to set the average voltage of the inverter over a time period Tow to be equal to the average voltage of the space vectors in that period [5].

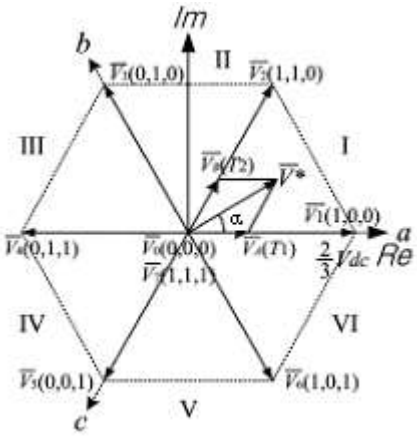


Fig.2. Determination of the Switching sequences in the three Phase inverter

In order to create the required rotating magneto-motive force in the stator of an AC induction machine the power inverter in Fig.1 needs to be driven with the correct switching variable vector [a,b,c]T. To do this, 3 main elements need to be addressed [3]:

1.1. Generating the Reference voltage vector

This requires precise positioning of the Reference voltage vector (V*) within the d-q plane shown in Fig.2. This implies accurately controlling the rotational speed, ω and magnitude of this vector, M.

1.2. Decomposing the reference voltage vector

In order to produce an arbitrary reference vector V*, a time average of given base vectors is required, i.e. the desired voltage vector V* located in a given sector, can be synthesized as a linear combination of the two adjacent base vectors, Vx and Vy, which are framing the sector, and one of the two zero vectors, hence:

$$V^* = dxV_x + dyV_y + dzV_z \quad (3)$$

Where Vz is the zero vector, and dx, dy and dz are the duty ratios of the states X, Y and Z within the PWM switching interval. The duty ratios must add to 100% of the PWM period, i.e.,

$$dx + dy + dz = 1 \quad (4)$$

Vector V* in Fig.2. can also be written as

$$V^* = MV_{max}e^{j\alpha} = dxV_x + dyV_y + dzV_z \quad (5)$$

Where M is the modulation index and α is the angle of the reference vector from the direct axis. By decomposing V* into its d-q components it can be shown that:

$$\frac{\sqrt{3}}{2} \times M\cos(\alpha) = dx + \frac{1}{2}dy \quad (6)$$

$$\frac{\sqrt{3}}{2} \times M\sin(\alpha) = \frac{\sqrt{3}}{2}dy \quad (7)$$

Solving for dx and dy gives:

$$dx = M \sin(60 - \alpha) \quad (8)$$

$$dy = M \sin(\alpha) \quad (9)$$

These same equations (8) and (9) apply to any sector, since the d-q reference frame, which has here no specific orientation in the physical space, can be aligned with any base vector. This is the reason why only a 60 degree sine lookup table is needed in this implementation.

1.3. *Realization of the switching pattern using PWM outputs*

By using the decomposed form of V*, appropriate duty ratios are calculated and these values are compared with either symmetrical or asymmetrical triangular wave according to the switching pattern.

2. SWITCHING PATTERNS

There are many switching patterns to implement space vector PWM. The pattern in Fig.3 is just one of them [1]. This switching pattern is fixed for each sector and can be summarized as 000 - Vi - Vi ± 60- 111 - Vi±60 - Vi -000, meaning the PWM outputs switch sequentially from 000 to Vi, Vi ± 60, 111, Vi ± 60, Vi, and back to 000 in each period, where Vi and Vi ± 60 are the basic space vectors forming the sector the reference voltage vector is in. Obviously, there are two possible switching directions for each sector, clock wise and counter clock wise. However, only one direction is allowed such that only one channel toggles at a time, except when the reference voltage vector is on one of the basic space vectors. This approach has chosen the switching direction for each sector that results in one channel toggling at a time, as shown in Fig.2. Therefore, once the sector of V* has been determined, the channels that toggle first, second and third are also determined The correct PWM output patterns are then generated by the compare logic

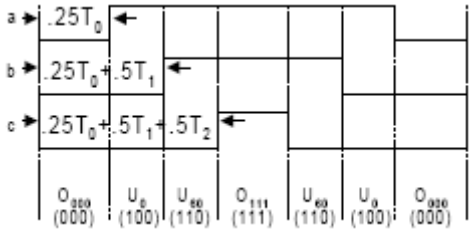


Fig.3.A symmetric space vector PWM switching pattern

All SVM schemes and most of the other PWM algorithms [8], use (3) and (4) for the output voltage synthesis. The modulation algorithms that use non-adjacent state space vectors have been shown to produce higher Total Harmonic Distortion (THD) and/or switching losses and are not analyzed here. The duty cycles dx, dy, and dz, are uniquely determined from Fig.2, using (3) and (4). The only difference between PWM schemes that use adjacent vectors is the choice of the zero vector(s) and the sequence in which the vectors are applied within the switching cycle [8].
The degrees of freedom we have in the choice of a switching pattern are:

- The choice of the zero vector - whether we would like to use V7(111) or V8(000) or both,
- Sequencing of the vectors
- Splitting of the duty cycles of the vectors without additional commutations.

II. IMPLEMENTATION OF SVPWM IN FPGA

Design methodology based on reuse modules
For very complex designs, modular conception is generally used to reduce design cycle. This methodology is based on hierarchy and regularity concepts. Hierarchy is used to divide a large or complex design into sub-parts called modules that are more manageable. Regularity is aimed to maximize the reuse of already designed modules.

With the ceaseless increasing progress of CAD tools, the improvement in terms of development time reduction lies more in the capacity of the designer to know how to classify and reuse his module models than in a perfect knowledge of his CAD tools. Nowadays, the manufacturers and the designers of circuits even propose to recover in free or restricted access, several design models, also called Intellectual Property IP modules. Besides, the complexity of some modules can be important as for the processor-cores. This design approach is then based on the reusability of IP modules.
We understand per module, an element of a library, available to the designer that can be directly inferred without having to design it. Therefore, the reuse methodology consists in selecting, throughout the synthesis process, the elements of a library that are useful for the design. These modules, extracted of the design flow, are distributed between the various levels of abstraction. The procedure of doing so is very similar to those used in DSP development with soft-macros.

This implementation contains 8 modules in FPGA namely

1. Speed variation depends up on the given push button input

2. Calculation of modulation index and step value (Δalpha)

3. Clock divider

4. Calculation of Ta, Tb, To

5. Calculation of number of 100 MHZ pulses for ON time pulse duration for six SCRs.

6. PWM for Thyristor 1 and Thyristor 4

7. PWM for Thyristor 2 and Thyristor 5

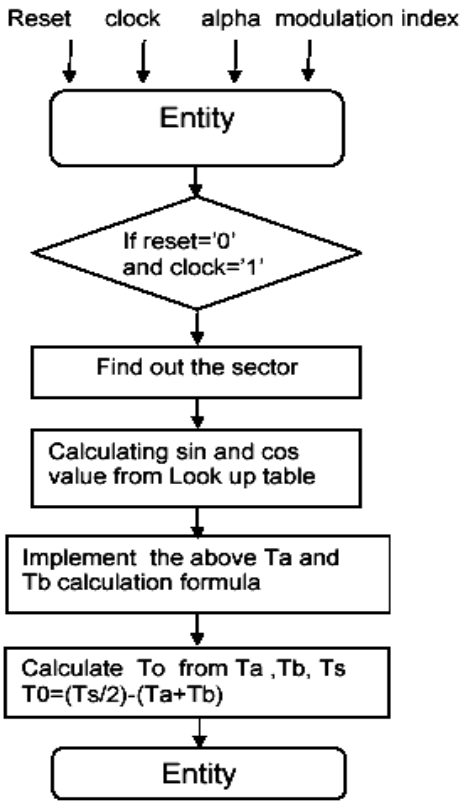
8. PWM for Thyristor 3 and Thyristor 6

TABLE II
Sector Calculation Table

p h	Sect or 1	Sect or 2	Sect or 3	Sect or 4	Sect or 5	Sect or 6

as e						
P h A	Ta+ Tb+ To/2	Tb+ To/2	To/2	To/2	Tb+ To/2	Ta+ Tb+ To/2
P h B	Tb+ To/2	Ta+ Tb+ To/2	Ta+ Tb+ To/2	Tb+ To/2	To/2	To/2
P h C	To/2	To/2	Tb+ To/2	Ta+ Tb+ To/2	Ta+ Tb+ To/2	Tb+ To/2

For page limiting, below flowchart explain only calculating Ta, Tb, To.



Different combinations of Ta, Tb and To/2 decide the no of 100 MHz clock pulses for ON period. ON Period Time calculation for each phase varies for every sector and it is calculated as given in table

IV.FPGADESIGN CONSIDERATIONS

The design flow of FPGA is different from that of microprocessor and DSP systems, as listed in Table II. FPGA demonstrates good performance and logic capacity by exploiting parallelism [S]. At present, a single FPGA platform can play multi-functions, including control, filter, and system I/O interface.

TABLE III
Comparison of FPGA AND DSP

IC	FPGA	DSP
Architecture	Distributed resource (look-up table,register,multiplier, memory)	Serial processing
Language	VHDL, Verilog	C, C++, Assembly
methodology	Synthesis,map,place,	Compile, link

The FPGA design flow is a three-step process consisting of design entry, implementation, and verification stages, as Shown in Fig. 6. The full design flow is an iterative process of entering, implementing, and verifying the design until it is correct and complete [6][7].

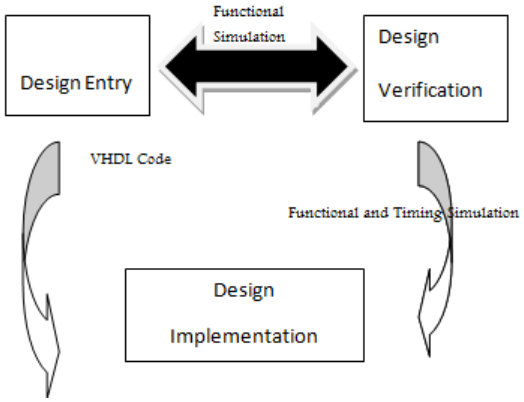


Fig 9. Design and Implementation flow

In realizing the proposed PWM Pattern generator, cost consideration led to selecting a Spartan -11 XC2SlOO-5PQ208 FPGA device from Xilinx Inc. This FPGA chip contains up to 100,000 logic gates, 600 configurable logic blocks (CLBs), and 196 input/output blocks (IOBs) [9]. It can be operated up to 200 MHz, while in the user board, the FPGA is actually operated at 30 MHz by using an external user-defined clock (DS1073). The resulting time resolution is33 ns. A 20 kHz PWM switching signal has a switching period of 50 us, this time resolution corresponds to a 0.07%error, which is neglectable.The design entry is text-based using VHDL language programs, there are one top-level module(modulator-top.vhd) and 8 sub-level modules (div-20.vhd,hex2lcd.vhd, led-mux.vhd, monostable.vhd, pwm-deadtime.vhd, section-time.vhd, sv-lut.vhd,elk-sw.vhd). A test-bench program is also created using the Model SIM VHDL Bencher tools.

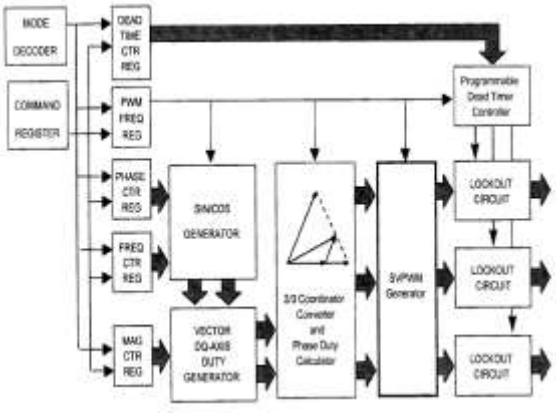


Fig 6 Functional block diagram of the programmable FPGA-based SVPWM IC.

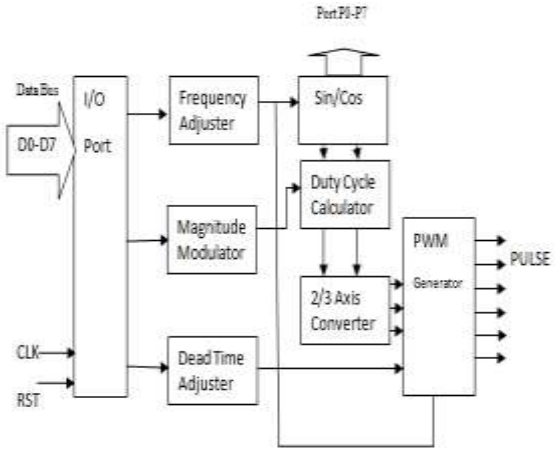


Fig. 14. Pin assignment of the FPGA-based SVPWM IC.

V.DESIGN VERIFICATION AND TEST RESULTS

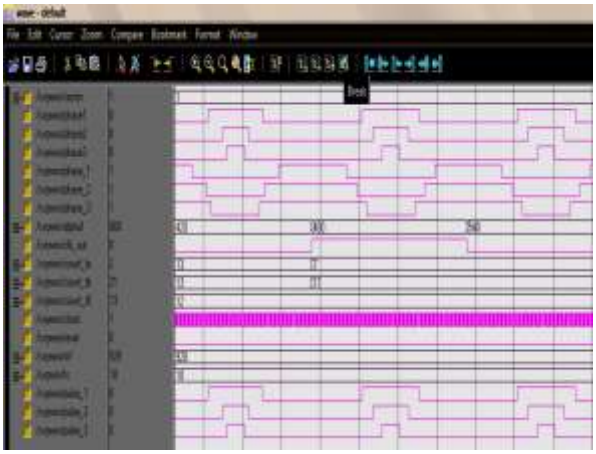


Fig.7 The simulation results for sector 1 using modelsim5.4se-ee

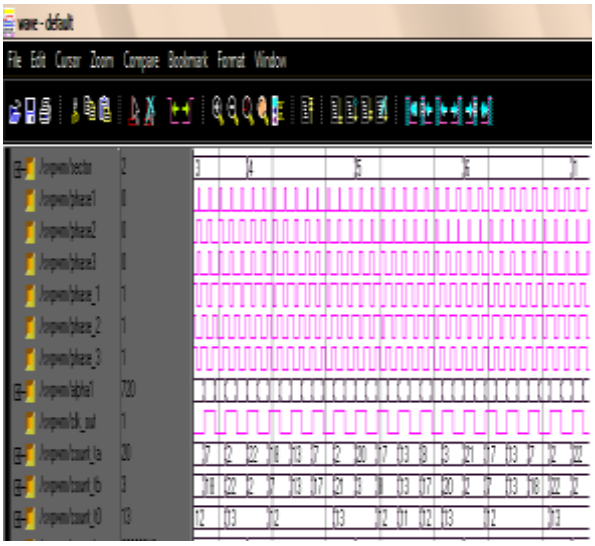


Fig.8 The simulation results for SVPWM - modelsim5.4se-ee

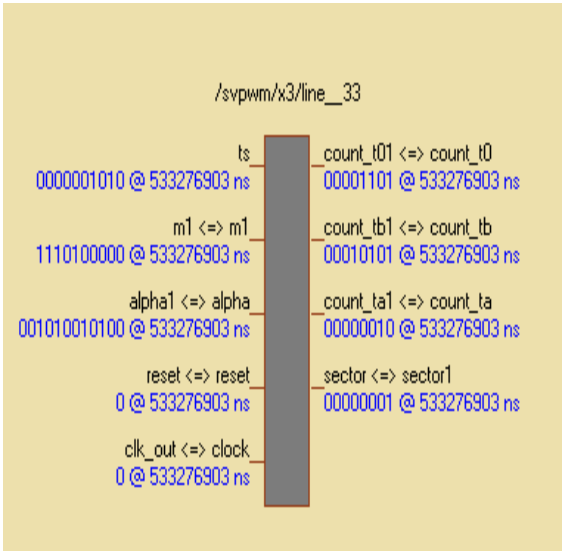


Fig 9. SVPWM IP Core – IC

VI.EXPERIMETAL SET UP

Fig 9. Shows the experimental setup in the FPGA. Xilinx project navigator tool is used for download the program into the Spartan device. SPARTAN device is fix the picky back board. The board contains the 4X4 matrix switches .these switches can be used for increasing and decreasing the speed. IPM module is a intelligent power module .IPM module act as both three phase inverter and chopper. So it can be able to drive both DC as well as AC motor individually.

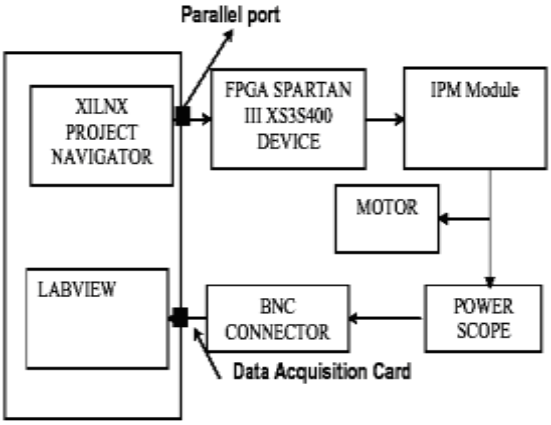


Fig 9. Experimental setup in the FPGA

V. CONCLUSION

The basic modules necessary for the vector control of Induction Motor namely SVPWM generator, Park's and Inverse Park's Transformation and digital PI Controller have been coded in VHDL and simulated. The same were downloaded into a Spartan III FPGA individually and the results are to be compared with existing schemes in terms of speed and memory occupied. As these modules are realized as hardware instead of sequential program to be executed in a processor the speed of execution will be incomparable. The tools used forth simulation; synthesis and realization are FPGA advantage from Mentor Graphics and Xilinx IS foundation series. The future enhancement of this work is to implement the digital Control Technique (Vector Control) on a Single Chip integrated with application specific processor which results in System on a Programmable Chip (SOPC). The SOPC proposal is being supported by AlteraSemiconductors with their Nios II soft core processor contest.

ACKNOWLEDGMENT
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