Monte Carlo Analysis of Propagation Delay Deviation due to Process Induced Line Parasitic Variations in Global VLSI Interconnects

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ABSTRACT
Process variation has recently emerged as a major concern in the design of circuits including interconnect in current nanometer regime. Process variation leads to uncertainties of circuit performances such as propagation delay. The performance of VLSI/ULSI chip is becoming less predictable as MOSFET channel dimensions shrinks to nanometer scale. The reduced predictability can be ascribed to poor control of the physical features of devices and interconnects during the manufacturing process. Variations in these quantities maps to variations in the electrical behavior of circuits. The interconnect line resistance and capacitance varies due to changes in interconnect width and thickness, substrate, implant impurity level, and surface charge. This paper provides an analysis of the effect of interconnect parasitic variation on the propagation delay through driver-interconnect-load (DIL) system. The impact of process induced variations on propagation delay of the circuit is discussed for three different fabrication technologies *i.e* 130nm, 70nm and 45nm. The comparison between three technologies interestingly shows that the effect of line resistive and capacitive parasitics variation on propagation delay has almost uniform trend as feature size shrinks. However, resistive parasitic variation in global interconnects has very nominal effect on the propagation delay as compared to capacitive parasitics. Propagation delay variation is from 0.01% to 0.04% and -4.32% to 18.1% due to resistive and capacitive deviation of -6.1% to 25% respectively.

Keywords
Process variation, interconnects, VLSI, parasitic, propagation delay.

1. INTRODUCTION
The device dimensions of VLSI chips have been aggressively reduced in the quest for improved speed, power, silicon area and cost characteristics [1-3]. Semiconductor technologies with feature sizes of several tens of nanometers are currently under development. As per, International Technology Roadmap for Semiconductors (ITRS) [4], the future nanometer regime circuits will contain more than ten billion MOSFETs and will operate at clock speeds well over 20GHz. It is now undoubtedly understood that distribution of robust and reliable power and ground lines; clock; data and address; and other control signals through interconnects in such a high-speed, high-complexity environment, is a tough task. The overall performance of any high-speed chip is extremely dependent on the interconnects, which connect different macro cells within a chip [5-8].

Due to ever increasing integration density and clock frequency, uncertainties linked with parameter variations emerge as a primary concern for VLSI chip design, especially in nanometer regime. Aggressive scaling of CMOS technology in sub-130-nm nodes has created huge challenges. Typically, the source of variations includes process-induced and environmental variations. The main sources of random process variation are random dopant fluctuation (RDF), line edge roughness (LER) and oxide thickness variation (OTV). Variations due to fundamental physical limits, such as RDF and LER, are increasing significantly with technology scaling [9-11]. Moreover, manufacturing tolerances in fabrication processes are not scaling at the same speed as the transistor's channel length, due to process control limitations (e.g., subwavelength lithography) [9-11]. Therefore, within-die statistical process variation deteriorates with succeeding technology generations. This paper considers the effect of process-induced line parasitic variations on propagation delay.

Today, semiconductor industry is facing a major challenge of variability [9]. In addition, digital circuits show an increased sensitivity to process variations due to low-power and low voltage operation requirements, which can result in failing to meet timing constraints. The on-going reduction of feature size goes together with an increase of variability. Obviously, there are more technological opportunities for aggressive scaling when more variability can be tolerated. This will lead to better and cheaper products (provided the quantities are large enough). Therefore, while the challenge of the technologists is to realize scaling while controlling the variability and the challenge of designers is to make the resulting variability sufficiently harmless by using suitable architectures and topologies, the challenge of Electronic Design Automation (EDA) is to provide accurate and efficient procedures to enable designers to understand the effect of the pertinent process variability on their design. Increasing process variations can affect electrical parameters of interconnects (e.g. capacitances) and further influence circuit performance and functionality.

Due to the process variation, interconnect technology parameters (ITP) are varying substantially. For the sake of simplicity, the researchers consider variations in metal thickness, metal width and interlayer dielectric thickness. The typical distribution of interconnect technology parameters can be observed for permittivity, inter level dielectric thickness, metal height and metal width [10]. The variation is especially large in the ILD (Inter Level Dielectric) thickness and metal line width. Their variations have a definite impact to the total line capacitance and

interline coupling capacitance and result in variation of the signal delay.

1.1 On Chip Interconnect Variations

The source for on chip variations (OCV) are concerned to variation in interconnect width and height, resulting in variation in both resistance and capacitance. Since the delays ascribed to interconnect are becoming more dominant as geometries shrink, particular consideration should be made for accurate analysis of interconnect variations. In advanced interconnect processes, that would involve the use of multiple dielectrics, and different metallization on different layers could result in noteworthy variations. Erosion is the additional means for variations and is a function of line space and density. Two additional sources of variation are the Chemical Mechanical Polishing (CMP) process and proximity effects in the photolithography and etch processes. Variation in the CMP process results from the difference of hardness of the interconnect material and that of the dielectric. Ideally the CMP process will remove the unwanted Copper, leaving only lines and vias. The photolithography and etch proximity effects are shown in micro loading effects as the etch process step tends to over-etch isolated lines. Diffraction effects and local scattering in photolithography may tend to over expose densely spaced lines and under expose isolated lines. Tiling and metal slotting have been added as design rule requirements to mitigate these effects by minimizing the density gradient. Different tiling algorithms will give varying results, but the smaller the density gradient, the smaller the variations that will be seen on the die [12].

2. INTERCONNECT MODELS

An interconnect can be modeled as either lumped or distributed form of RC (resistance-capacitance) or RLC (resistance-capacitance-inductance). In deep submicron technology, lumped models are no longer capable of satisfying the accuracy requirements. It is well accepted that simulations of a distributed RC model of an interconnect matches more accurately the actual behavior in comparison to lumped RC model [5-8]. In similar fashion, a distributed RLC model outperforms the lumped RLC model in terms of modeling accurately the behavior of a line. A distributed RLC model of an interconnect, known as the transmission line model, becomes the most accurate approximation of the actual behavior [5]. The transmission line analogy for an interconnect considers the signal propagation to be a wave propagation over the interconnect medium. This is in contrast to the distributed RC model, where the signal diffuses from source to the destination governed by the diffusion equation. In the wave mode, a signal propagates by alternatively transferring energy from the electric to magnetic fields, or equivalently from capacitive to the inductive nodes. Interconnect models must incorporate distributed self and mutual inductance to accurately estimate interconnect time delay, power dissipation, crosstalk and other parameters of significance.

The evolution of various models with time is shown in Figure 1. It is assumed that leakage conductance 'g' equals 0, which is true for most insulating materials such as SiO2, sapphire etc. Dealing with inductance requires efficient extraction methods. Presence of inductance also increases the processing time of the computer-aided design tools. Usually the interconnect circuits extracted from layouts contain a large number of nodes that make the simulation highly CPU intensive. Distributed coupled RLC models become necessary even for the early design stages.

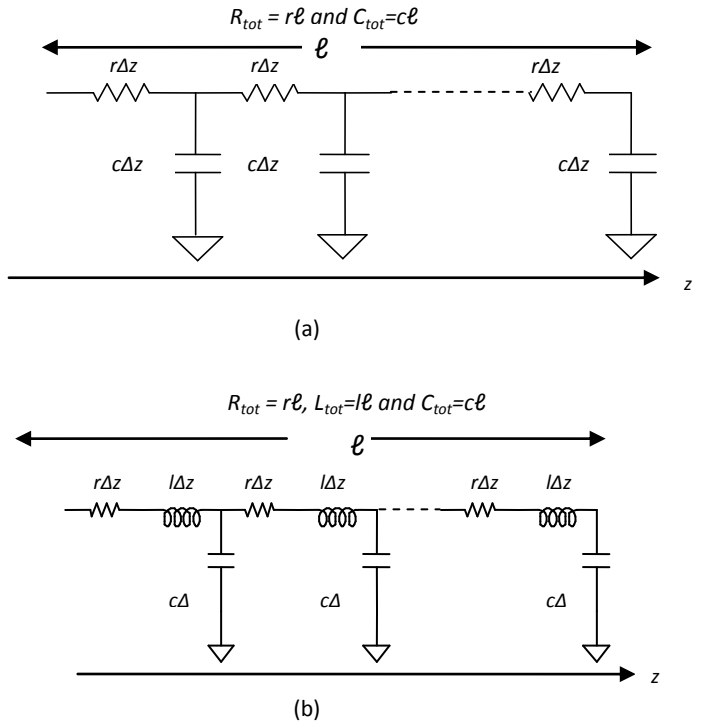

Figure 1 Development of interconnect models (a) RC model; (b) RLC model.

3. MONTE CARLO ANALYSIS OF DIL SYSTEM

The analysis carried out in this work takes into account a Driver-Interconnect-Load (DIL) system as shown in Figure 2. The driver is an inverter gate driving the interconnect. The propagation delay of a DIL system is dependent on various physical parameters which are prone to process variation. In this analysis, the driver is subjected to process variations for three different technologies of 130nm, 70nm and 45nm. To obtain statistical information on how much the characteristics of a circuit can be expected to scatter over the process, Monte Carlo analysis is applied. Monte Carlo analysis performs numerous simulations with different boundary conditions. It chooses randomly different process parameters within the worst case deviations from the nominal conditions for each run and allows statistical interpretation of the results. In addition to the process parameter variations, mismatch can be taken into account as well, providing a more sophisticated estimation of the overall stability of the performance with respect to variations in the processing steps. In most cases the parameters on which the assumptions for the mismatch are based are worst case parameters. A proper layout and choice of devices can significantly improve scatter due to mismatch. In order to obtain reasonable statistical results, a large number of simulations are needed, leading to quite long simulation times. Using Monte Carlo simulations, this work analyzes the effect of resistive and capacitive line parasitic variation of interconnect due to process variation on the propagation delay of DIL system. The propagation delay variations through DIL system are observed for process variations in three different technologies.

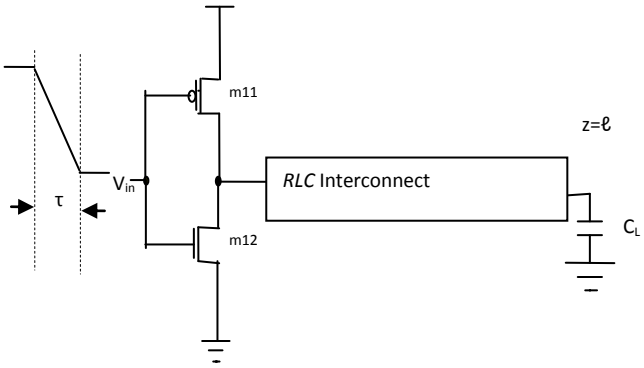

Figure 2 Driver Interconnect Load (DIL) System

4. RESULTS AND DISCUSSION

Monte Carlo simulation results were observed for deviation in propagation delay with change in line parasitics. Table-I shows variation in propagation delay due to deviations in capacitance for 130nm, 70nm and 45nm fabrication technologies. It is clearly observed that the variation in propagation delay is almost same for all process technologies of 130nm, 70nm and 45nm. These results which can also be noticed in figure 3, are in sharp contrast to observations made in previous research works related to process variations in oxide thickness [13], driver width [14], and threshold variations [15]. Previously, it was observed that in presence of significant variations of device model parameters the variations in performance parameter such as delay is severely affected. The comparison between different technologies showed that as feature size shrinks the process variation becomes a dominant factor and subsequently raises the variation in delays. Contradictorily, as per the results observed in this work it is observed that although the deviation in delay is more pronounced with increase in line capacitance variation, but these variations have almost same magnitude as the process technology changes from 130nm to 45nm. The delay variations are from -4.32% to 18.1 % due to capacitive deviation of -6.1% to 25%.

Table-1 Variation in propagation delay due to deviation in capacitance for 130nm, 70nm and 45nm fabrication technology

% Variation in capacitance	Propagation Delay Variation (130nm)	Propagation Delay Variation (70nm)	Propagation Delay Variation (45nm)
-6.08	-4.64	-4.65	-4.32
-2.43	-1.87	-1.88	-1.77
-2.33	-1.79	-1.8	-1.69
-0.29	-0.2	-0.22	-0.21
1.19	0.83	0.9	0.86
2.6	1.82	1.94	1.93
5.28	3.71	3.93	3.92
5.53	3.87	4.12	4.1
7.63	5.3	5.63	5.62
24.92	17.93	18.53	18.1

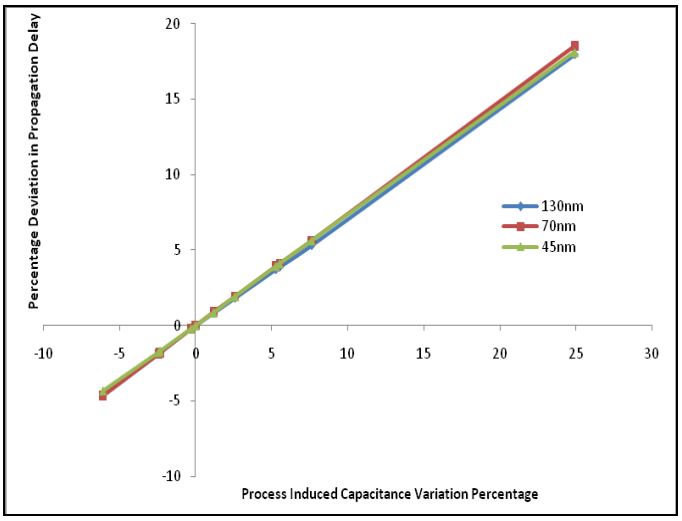

Figure 3-Plot showing percentage deviation in propagation delay with respect to process induced capacitance variation.

Now, Table-II shows variation in propagation delay due to deviations in resistance for different fabrication technologies. It is demonstrated that the variation in propagation delay is almost same for all process technologies. These results as also shown in figure 4, are again in sharp contrast to observations made by previous research works where the variations in performance parameter such as delay is severely affected with reduction in feature size for higher technologies. Previous researches illustrated that with shrinking feature sizes process variation turned out to be dominant and subsequently raised the variation in delays. Contradictorily, our results observes that the deviation in delay is extremely small for variation of line resistance even upto 25% in global VLSI interconnects domain. Moreover, these variations are in same magnitude as the process technology changes from 130nm to 45nm. The delay variations were from -0.01% to 0.04 % due to resistive deviation of -6.1% to 25%.

Table-II Variation in propagation delay due to deviation in resistance for 130nm, 70nm and 45nm fabrication technology

% Variation in Resistance	Propagation Delay Variation (130nm)	Propagation Delay Variation (70nm)	Propagation Delay Variation (45nm)
-6.09	-0.01	-0.01	-0.01
-2.44	0	0	0
-2.33	0	0	0
-0.29	0	0	0
1.19	0	0	0
2.6	0	0.01	0.01
5.29	0.01	0.01	0.01
5.53	0.01	0.01	0.01
7.63	0.01	0.01	0.01
24.92	0.04	0.04	0.04

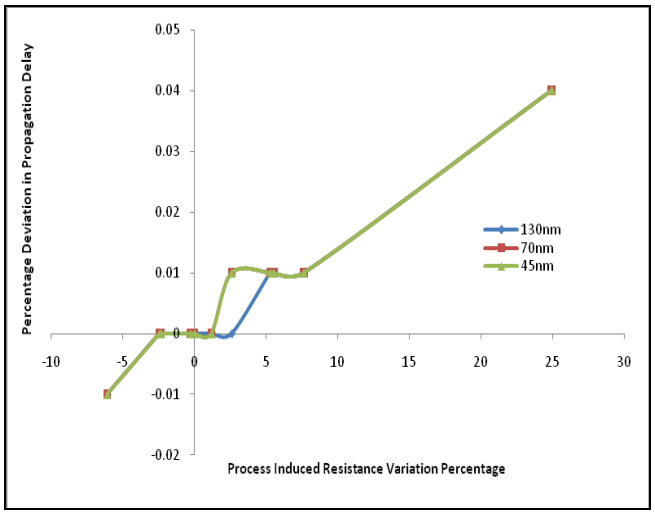

Figure 4-Plot showing percentage deviation in propagation delay with respect to process induced resistance variation

4. CONCLUSION

This research work evaluated the effect of process induced interconnect resistive and capacitive parasitic deviation on propagation delay. These effects were observed for process corners of 130nm, 70nm and 45nm technologies. Monte Carlo simulations were run using distributed driver-interconnect-load model. The comparison between three technologies interestingly demonstrated that the effect of line resistive and capacitive parasitic variation on propagation delay has almost uniform trend as device size shrinks. However, resistive parasitic variation in global interconnects has very nominal effect on the propagation delay as compared to capacitive parasitics. Propagation delay variation is from 0.01% to 0.04% for a variation of line resistance from -6.1% to 25%. Similarly the delay variations were from -4.32% to 18.1 % due to capacitive deviation of -6.1% to 25%.

5. REFERENCES

[1] Mizuno, T., Okumtura, J., and Toriumi, A. 1994. "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2216–2221.

[2] Frank, D., Dennard, R., Nowak, E., Solomon, P., Taur, Y. and Wong H.-S. 2001. "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–288.

[3] Croon, J., Decoutere, S., Sansen, W. and Maes H. 2004. "Physical modeling and prediction of the matching properties of MOSFETs," in *Proc. 34th ESSDERC*, pp. 193–196.

[4] "The International Technology Roadmap for Semiconductors," *ITRS Website*. [Online]. Available: http://public.itrs.net

[5] Kaushik, B. K., Sarkar S. and Agarwal R.P. 2007. "Waveform Analysis and Delay Prediction for a CMOS Gate Driving RLC Interconnect Load", *Integration, the VLSI Journal*, Elsevier Pub., Netherlands, vol. 40, no. 4, pp. 394-405.

[6] Kaushik, B. K. and Sarkar S. 2008 "Crosstalk Analysis for a CMOS-Gate-Driven Coupled Interconnects" *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 6, pp. 1150-1154.

[7] Kaushik, B. K., Sarkar S., Agarwal R. P., and Joshi R. C., 2009 "Crosstalk Analysis of Simultaneously Switching Interconnects" *International Journal of Electronics*, Taylor and Francis (UK), vol. 96, no.10, pp. 1095-1114.

[8] Kaushik, B. K., Sarkar S., Agarwal R. P. and Joshi R. C., 2007. "Effect of Line Resistance and Driver Width on Crosstalk in Coupled VLSI Interconnects" *Microelectronics International*, Emerald Pub. U.K., vol. 24, no. 3, pp. 42-45.

[9] Masuda, H., Ohkawa, S., Kurokawa, A. and Aoki, M., 2005. "Challenge: Variability characterization and modeling for 65- to 90-nm processes," in *Proc. CICC*, pp. 593–599.

[10] Boning, D. and Nassif, S., 2001. "Models of process variations in device and interconnect," in *Design of High Performance Microprocessor Circuits*, A. Chandrakasan, W. J. Bowhill, and F. Fox, Eds. New York: Wiley.

[11] Verma, K. G., Kaushik, B.K. and Singh, R., 2009. "Effects of Process Variation in VLSI Interconnects- a Technical Review" *Microelectronics International*, Emerald Pub. U.K., vol. 26, no. 3, pp. 49-55.

[12] Jarrar, A. and Taylor, K., 2006. "On-Chip Variation and Timing Closure", Electronics Design, Strategy, News (EDN), June, 2006.

[13] Verma, K.G., Kaushik, B.K. 2010. "Effect of Process Based Oxide Thickness Variation on the Delay of DIL System Using Monte Carlo Analysis" *International Journal of Recent Trends in Engineering*. Academy Publishers, Finland, vol. 3, no. 4, pp. 27-31.

[14] Verma, K.G., Kaushik, B.K., Singh, R. 2010. "Propagation Delay Variations under Process Deviation in Driver Interconnect Load System," *International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom)*, pp.408-410.

[15] Verma, K.G., Kaushik, B.K. and Singh, R. 2010. "Propagation Delay Variation due to Process Induced Threshold Voltage Variation" *Communications in Computer and Information Science, 1, Information and Communication Technologies*, Springer, vol.101, Part 3, pp. 520-524.