Speed Comparison of 16x16 Vedic Multipliers

Manoranjan Pradhan
VSS University of Technology
Burla, Sambalpur
Orissa, India-768018

Rutuparna Panda
VSS University of Technology
Burla, Sambalpur
Orissa, India-768018

Sushanta Kumar Sahu
VSS University of Technology
Burla, Sambalpur
Orissa, India-768018

ABSTRACT

The paper presents the concepts behind the "Urdhva Tiryagbhyam Sutra" and "Nikhilam Sutra" multiplication techniques. It then shows the architecture for a 16×16 Vedic multiplier module using Urdhva Tiryagbhyam Sutra. The paper then extends multiplication to 16×16 Vedic multiplier using "Nikhilam Sutra" technique. The 16×16 Vedic multiplier module using Urdhva Tiryagbhyam Sutra uses four 8×8 Vedic multiplier modules; one 16 bit carry save adders, and two 17 bit full adder stages. The carry save adder in the multiplier architecture increases the speed of addition of partial products. The 16×16 Vedic multiplier is coded in VHDL, synthesized and simulated using Xilinx ISE 10.1 software. This multiplier is implemented on Spartan 2 FPGA device XC2S30-5pq208. The performance evaluation results in terms of speed and device utilization are compared with earlier multiplier architecture. The proposed design has speed improvements as compared to multiplier architecture presented in [5].

General Terms

Algorithms.

Keywords

Vedic Multiplier, Nikhilam Sutra, Urdhva Tiryagbhyam Sutra, VHDL, FPGA.

1. INTRODUCTION

Vedic mathematics was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). Ancient Indian system of mathematics was derived from Vedic Sutras. The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics. The Vedic algorithms can be applied to arithmetic, trigonometry, plain and spherical geometry, calculus.

In [1], authors have proposed a new multiplier based on an Vedic algorithm for low power and high speed applications. Their multiplier architecture is based on generating all partial products and their sums in one step. They claim that their proposed Vedic multiplier is faster than the corresponding array multiplier and Booth multiplier. The authors in [2] have tested and compared various multiplier implementations such as Array multiplier, Multiplier macro, Vedic multiplier with full partitioning, Vedic multiplier using 4 bit macro, fully Recursive Vedic multiplier, Vedic multiplier using 8 bit macro for optimum speed. They have claimed that Vedic method is not fundamentally different from conventional method of multiplication.The implementation of Rivest, Shamir & Adleman (RSA) encryption/decryption algorithm using Vedic mathematics is proposed to improve performance in [3]. They have used Vedic multiplier and division architecture in the RSA circuitry for improved efficiency. Their results show that RSA circuitry implemented using Vedic division and multiplication is efficient in terms of area/speed compared to its implementation using conventional multiplication and division architectures. Dhillon and Mitra [4] proposed a multiplier using 'Urdhva Tiryagbhyam' algorithm, which is optimized by 'Nikhilam' algorithm. They have suggested a reduced bit multiplication algorithm using 'Urdhva Tiryakbhyam' and 'Nikhilam' Sutra.

We have developed a new Vedic multiplier structure using 'Nikhilam' Sutra. The carry save adder implemented in the proposed architecture reduces propagation delay significantly. It is believed that our architecture may set new path for future research.

2. Vedic Multiplier using 'Urdhva Tiryagbhyam'Sutra

The 'Urdhva Tiryagbhyam' Sutra [5-10] is a general multiplication formula applicable to all cases of multiplication. 'Urdhva' and 'Tiryagbhyam' words are derived from Sanskrit literature. 'Urdhva' means "Vertically" and 'Tiryagbhyam' means "crosswise".

The multiplication of two 2-digit decimal numbers 21 and 32 is shown in Figure 1. The least significant digit 1 of multiplicand is multiplied vertically by least significant digit 2 of the multiplier, get their product 2 and set it down as the least significant part of the answer. Then 2 and 2, 1 and 3 are multiplied crosswise, add the two, get 7 as the sum and set it down as the middle part of the answer. Then 2 and 3 is multiplied vertically, get 6 as their product and put it down as the last the left hand most part of the answer.

So 21 × 32 = 276.

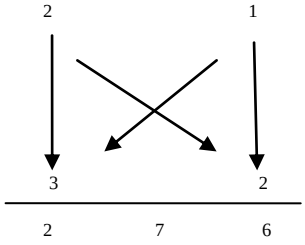

Fig 1: Multiplication of 21×32 by 'Urdhva Tiryagbhyam' Sutra.

The 'Urdhva Tiryagbhyam' algorithm can be implemented for binary number system in the same way as decimal number

system. Let us consider the multiplication of two 2-bit binary numbers a1a0 and b1b0. Assuming that the result of this multiplication would be 4 bits, we express it as p2 p1 p0. The least significant bit a0 of multiplicand is multiplied vertically by least significant bit b0 of the multiplier, get their product p0 and set it down as the least significant part of the answer (p0). Then a1 and b0, and a0 and b1 are multiplied crosswise, add the two, get sum1 and carry1, the sum bit is the middle part of the answer (p1). Then a1 and b1 is multiplied vertically, and add with the previous carry (carry1) and get p2 (2 bit) as their product and put it downs as the left hand most part of the answer (p2). So a1a0 X b1b0=p2 p1 p0.Similarly The 2×2 Vedic multiplier module is then used to implement higher level multipliers (4×4 multiplier, 8×8 multiplier, 16×16 multiplier).

2.1 16x16 Vedic Multiplier Module

The architecture of 16x16 Vedic multiplier using 'Urdhva Tiryagbhyam' Sutra is shown in Fig.2. The 16x16 Vedic multiplier architecture is implemented using four 8x8 Vedic multiplier modules, one 16 bit carry save adder, and two 17 bit binary adder stages.

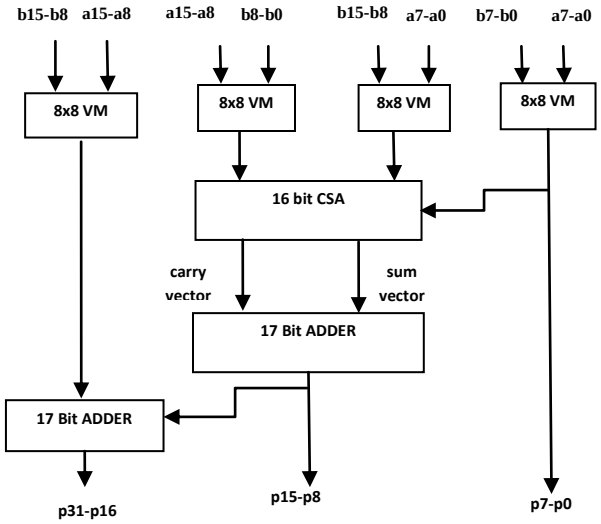

Fig 2: Architecture of 16x16 Vedic Multiplier'Urdhva Tiryagbhyam' Sutra.

Multiplication Result = (p31-p16) & (p15-p8) & (p7-p0). Where & = concatenate operation.

The proposed architecture uses 16-bit carry save adder and 17-bits adder modules to generate the final 32-bits product (p31-p16) & (p15-p8) & (p7-p0).The p7- p0 (8-bits) of the product represents least significant 8-bits of the 16-bit output of the right hand most 8x8 multiplier module. The 16-bit carry save adder adds three input 16-bit operands i.e. concatenated 16-bit ("00000000" & most significant eight bits output of right hand most 8x8 multiplier module), each 16-bit output of second and third 8x8 multiplier modules. The 16-bit carry save adder produces two 16-bit output operands, sum vector and carry vector. The outputs of the carry save adder are fed into first 17-bit adder to generate 17-bit sum. The middle part (p15- p8) represents the least significant eight bits of 17-bit sum. The 16-bit output of the left most 8x8 multiplier module and concatenated 16-bits ("0000000"& the most significant nine bits of 17-bits sum) are fed into second 17-bit adder. The p31-p16 represents sixteen bit sum. The 33rd carry bit is omitted while taking the final product.

3. PROPOSED 16X16VEDIC MULTIPLIER USING NIKHILAM SUTRA

The Nikhilam Sutra literally means "all from 9 and last from 10". It is more efficient when the numbers involved are large. The Nikhilam Sutra algorithm is efficient for multiplication only when the magnitudes of both operands are more than half their maximum values. For n-bit numbers, therefore both operands must be larger than 2n-1. Nikhilam Sutra is explained by considering the multiplication of two single digit decimal numbers 8 and 7 where the chosen base is 10 which is nearest to and greater than both these two numbers [6].

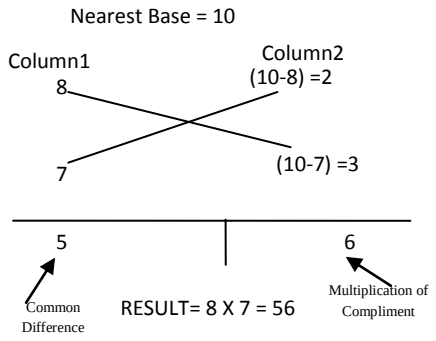

Fig 3: Multiplication of Two 1-Digit Decimal Numbers (8 x 7) using Nikhilam Sutra.

As shown in Fig.3, the multiplier and the multiplicand are written in two rows followed by the differences of each of them from the chosen base, i.e., their compliments. There are two columns of numbers, one consisting of the numbers to be multiplied (Column 1) and the other consisting of their compliments (Column 2). The product also consists of two parts which are demarked by a vertical line for the purpose of illustration. The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 i.e., (2x3=6). However the surplus portion on the RHS is carried over to Left. The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column 1 or vice versa, i.e., 8 -3 = 5 or 7-2 = 5. The final result is obtained by concatenating RHS and LHS (Answer = 56).

3.1 Nikhilam Sutra in Binary Number

The Nikhilam sutra can also be applicable to binary number system. The compliment of multiplicand or multiplier is represented by taking 2's compliment of that number. The right hand side part of the product is implemented using 16X16 bit multiplication. The left hand side part is implemented using 16-bit carry save adder. Hence the multiplication of two 16-bit numbers is reduced to the multiplication of their compliments and addition.

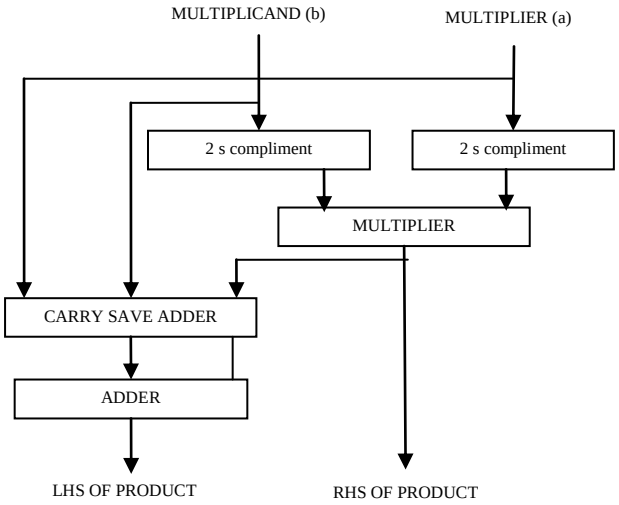

Fig.4: The Architecture of proposed 16x16 Vedic Multiplier using Nikhilam Sutra.

The Block Diagram of Multiplier using Nikhilam Sutra is shown in Fig.4.The two inputs 'a' and 'b' represents 16-bit multiplier operand and 16-bit multiplicand operand respectively. The compliment of multiplicand or multiplier is represented by taking 2's compliment of that number .So the 2's complement block produces the complemented output of 16-bit multiplier operand (- a) and 16-bit multiplicand operand ( ). The complemented output of 16-bit multiplier operand and 16-bit multiplicand operand are two inputs to multiplier. The number of bits required in the right hand side of the product should have 16- bits irrespective of the number of bits in the product of compliments. So the surplus 16-bits of the right hand side part of the product is fed to one of the input of carry save adder for left hand part of the result. The left hand side part is implemented using 16-bit carry save adder. The negative of complemented multiplicand is implemented by taking output of the 2's complement block in the left hand side. The three 16-bits input operands of carry saver are 16-bit multiplier, the negative of complemented multiplicand and the surplus 16-bits of the right hand side part of the product. The two output of carry save adder i.e. sum vector and carry vector are inputs to binary adder block. The output of the adder represents left hand side of the answer.

4. RESULTS AND DISCUSSION

Table-1 displays the comparison of synthesis results of the proposed 16x16 Vedic multiplier using Nikhilam Sutra with 16x16 Vedic multiplier using Urdhva Tiryagbhyam Sutra presented in [5].

It has been observed that for 16x16 Vedic multiplier module using Nikhilam Sutra , the gate delay is 33.729 ns with Device utilization (number of slices- 45%) while it is 41.751 ns with Device utilization (number of slices- 87%) for the 16x16 Vedic multiplier module using Urdhva Tiryakbhyam Sutra.

TABLE I. Comparison of Synthesis Results of proposed 16x16 Bit Vedic Multiplier with [5].

Device Spartan2 XC2S30: -5 pq208	16 x 16 Urdhva Tiryagbhyam Sutra [5]	Proposed 16x16 Nikhilam Sutra
Delay	41.751 ns	33.729 ns
Number of Slices	377 out of 432(87%)	198 out of 432(45%)
Number of 4-input LUTs	670 out of 864(77%)	387 out of 864(44%)
Number of bonded IOBs	64 out of 132(48%)	64 out of 132(48%)

Table-2 shows the synthesis reports of the proposed 16x16 Vedic multiplier using Nikhilam Sutra with 16x16 Vedic multiplier using Urdhva Tiryakbhyam Sutra.

TABLE 2. HDL Synthesis Report of 16x16 Bit Vedic Multiplier

16x16 Vedic Multiplier (Nikhilam Sutra)	16x16 Vedic Multiplier (Urdhva Tiryagbhyam Sutra)
# Adders : 4	# Adders : 42
16-bit adder : 3	16-bit adder : 1
17-bit adder : 1	17-bit adder : 1
# Xors : 1	4-bit adder : 16
16-bit xor3 : 1	5-bit adder : 16
	8-bit adder : 4
	9-bit adder : 4
	# Xors : 149
	1-bit xor2 : 128
	16-bit xor3 : 1
	4-bit xor3 : 16
	8-bit xor3 : 4

From Table-2, the 16x16 Vedic multiplier using Nikhilam Sutra found to use only four numbers of adders (three numbers of 16-bit adder and one number of 17- bit adder) and one 16-bit XOR gate. However, The 16x16 Vedic Multiplier implementation using 'Urdhva Tiryagbhyam' Sutra uses 42 numbers of adders, and 149 numbers of exclusive-OR gates. The 42 numbers of adders includes 16 numbers of 4-bit adders, 17 numbers of 5-bit adders, 4 numbers of 8-bit adders, 4 numbers of 9- bit adders, one 16-bit adder, and one 17-bit adder. The 149 numbers of exclusive-OR gates includes 128 numbers of 1-bit exclusive-OR, 16 numbers of 4-bit exclusive-OR , 4 numbers of 8-bit exclusive-OR and 1 number of 16-bit exclusive-OR. The 16x16-bit Vedic multiplier using Nikhilam Sutra implementation uses less numbers of adders and exclusive-OR gates compared

to16x16Vedic multiplier using 'Urdhva Tiryagbhyam' Sutra. The high propagation delay of 16x16 Vedic multiplier using 'Urdhva Tiryagbhyam' Sutra has been reduced significantly by using Nikhilam Sutra. Because Nikhilam Sutra reduces the multiplication of two large numbers into the multiplication of two small numbers and addition. Hence, there is significant speed improvement for 16x16 Vedic multiplier implementation using Nikhilam Sutra..

5. CONCLUSION

The proposed Vedic multiplier architecture shows speed improvements over multiplier architecture presented in [5]. The 16x16 Vedic multiplier using 'Nikhilam' Sutra found to be better than 16x16 Vedic multiplier using 'Urdhva Tiryakbhyam' Sutra in terms of speed when magnitude of both operands are more than half of their maximum values . This approach may be well suited for multiplication of numbers with more than 16 bit size.

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