Implementation of Delay and Power Monitoring Schemes to Reduce the Power Consumption

Pavan.T.K.
M.Tech. (VLSI Design)
T.N, India

Jagannadha Naidu.K
Asst.Prof, VIT University
T.N, India

Nagaraju.V
M.Tech, VIT University
T.N, India

ABSTRACT
As process technology shrinks, the adaptive leakage power compensation scheme will become more important in realizing high-performance and low-power applications. In order to minimize total active power consumption in digital circuits, one must take into account sub-threshold leakage currents that grow exponentially as technology scales. This describes to predict how dynamic power and sub-threshold power must be balanced. The exclusive supply voltage control switching makes stable operations. The threshold voltage control successfully maintains a ratio of switching to leakage current and which represents the reduced power consumption. The goal of this paper is to: i) Maintains the optimized body bias conditions. ii) Maintains the best power-delay tradeoff. The results with a 180-nm CMOS device explain that the proposed architecture causes in the successful optimization of power.

Keywords
CMOS, leakage current, supply voltage control, threshold voltage control, switching current.

1. INTRODUCTION
The effects of scaled V_{dd} and gate oxide tunneling leakage in order to achieve optimized body bias values in standby system. The dual V_{th} technique provides a practical way to achieve both high performance and low leakage power dissipation for current deep submicron technology. The V_{dd} was controlled to control the propagation delay in the chip core critical path. And in the chip core we can implement any design whatever we need based on the specification. The control of V_{th} was to compensate for V_{th} fluctuations, in order to avoid any oscillation problems. To determine the effects of process variations on the leakage reduction, two parameters will be varied and namely the gate length and BTBT current. Therefore, new junction engineering techniques to reduce the bulk Band-To-Band Tunneling leakage across the junction will be essential to preserve the performance. As the power monitoring scheme directly measures relative power from circuit.

This paper is summarized as follows. Section 2 describes the power monitoring schemes. Section 3 explains the block diagram of V_{dd}/V_{th} control system. Section 4 explains in detail our proposed delay and power monitors for the active mode, as well as standby mode. Section 5 shows Measurement results. Section 6 describes about the conclusion.

2. THE POWER MONITORING SCHEMES
2.1 Current consumption in Active mode
The active current equation of static CMOS described as the following equation.

$$I_{active}=I_{sw}+I_{leak} \quad (1)$$

Where I_{sw}=switching current and $I_{leak=}$leakage current.

2.2 The Principle of Power monitoring
Fig.1. gives the relationships among I_A, I_B and I_{SUM}. I_A and I_B are straight lines. I_{SUM} is the sum of I_A and I_B as described in the following equations:

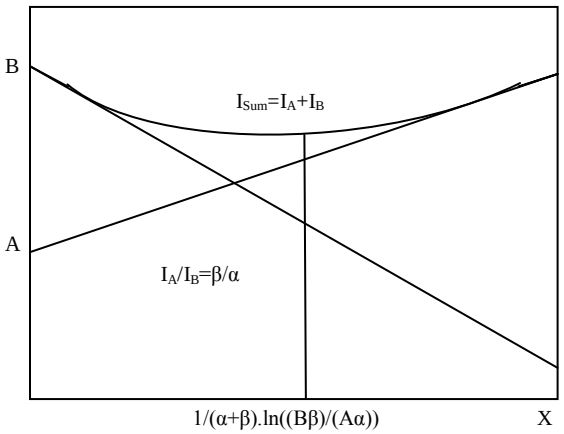

Figure 1: Relationships among I_A, I_B and I_{SUM}.

$$I_{SUM}(x)=I_A(x)+I_B(x) \quad (2)$$

Where $I_A(x)=A.\exp(\alpha x)$ and $I_B(x)=B.\exp(-\beta x)$.

Finally, x can be calculated as

$$I_{SUM}(x)'=A\alpha.\exp(\alpha x)-B\beta.\exp(-\beta x)=0 \quad (3)$$

Therefore,

$$x=1/(\alpha+\beta).\ln(B\beta/A\alpha) \quad (4)$$

The value of I_{SUM} can be determined as

$$I_A(x)/I_B(x)=\beta/\alpha \quad (5)$$

At the minimum value of I_{SUM}, the ratio I_A/I_B can be determined.

2.3 Current consumption in Standby mode

The leakage current in standby mode can be represented as the following equation.

$$I_{leak}=I_{subth}+I_{sub}+I_{dg} \quad (6)$$

Where I_{subth} is the sub-threshold current, I_{sub} is the substrate current and which is the sum of gate to bulk leakage and gate induced drain leakage. And I_{dg} is the drain-gate leakage current. The minimum I_{leak} will be achieved at $I_{subth}=I_{sub}$. While reverse body bias decreases I_{subth}, it increases I_{sub} and does not affect I_{dg}.

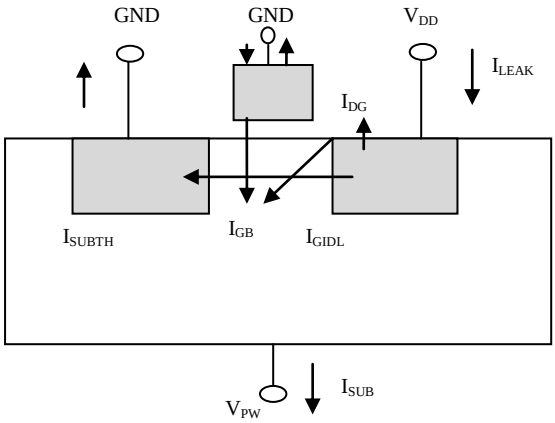

Figure 2: When the MOS is in OFF state.

Each leakage current depends on V_{DD}. Decreasing V_{DD} will reduce the value of leakage current components such as I_{SUB} and I_{DG}. The minimum value of I_{LEAK} gives a tradeoff between I_{SUBTH} and I_{SUB}.

3. V_{DD}/V_{TH} CONTROL SYSTEM DESIGN

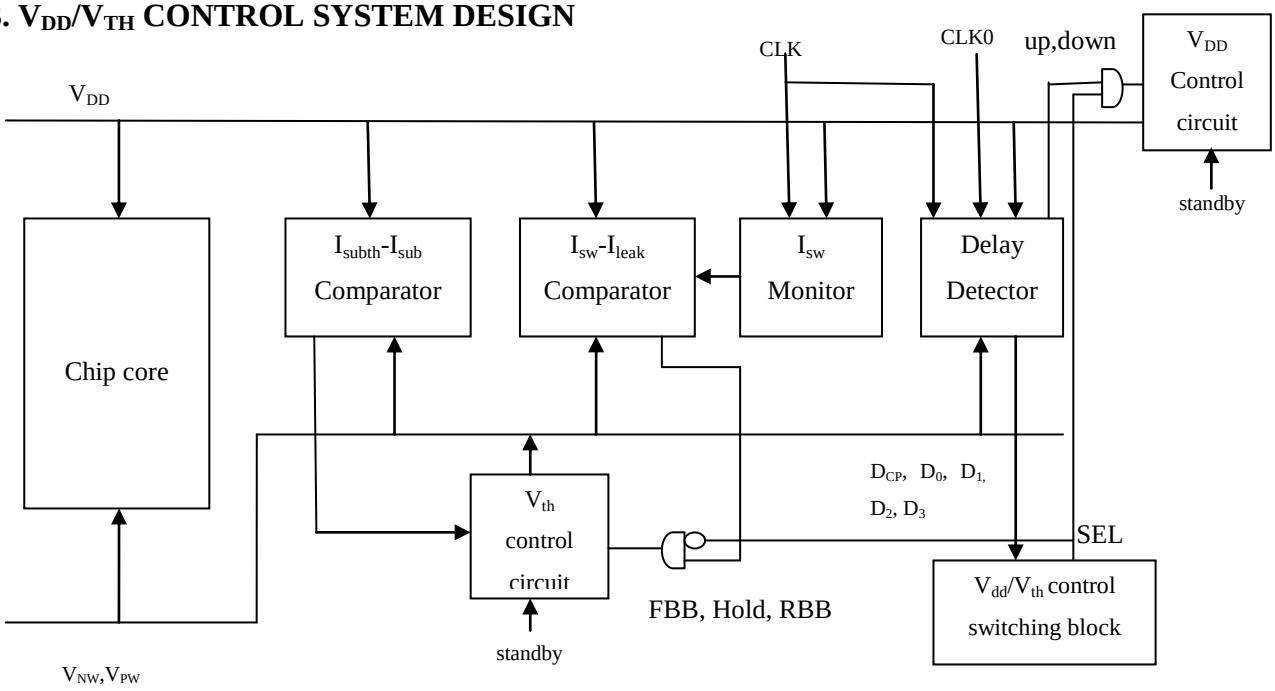

Figure 3: The Block Diagram of V_{dd}/V_{th} control system.

The above diagram explains in detail about the total block diagram of V_{dd}/V_{th} control system. It is necessary for a V_{DD}/V_{th} control system not only to achieve minimum power consumption but also to satisfy speed performance demands. V_{DD} control is highly sensitive and has wide speed control range. V_{th} control or V_{PW},V_{NW} control has low sensitivity with respect to speed and is highly sensitive with respect to sub-threshold leakage current.. Here V_{DD} control is used to help satisfy speed performance demands and V_{th} control to help achieve minimum power consumption, so as to maintain the desired I_{SW}/I_{leak} ratio. The V_{DD} and V_{th} control system is illustrated in the above figure. And it consists of four parts: i) V_{DD} controller. ii) V_{th} controller. iii) Delay monitor that contains a delay detector and a V_{DD}/V_{th} control switching block. iv) Power monitor that contains an I_{SW} monitor, I_{SW}-I_{leak} comparator and an I_{subth}-I_{sub} comparator. The V_{DD} controller supplies, on the basis of delay monitoring results, the minimum voltage at which the chip can operate for a given clock frequency at a certain V_{th}. The V_{th} controller supplies, on the basis of power monitoring results, the optimum body bias at which the chip consumes minimum power at a certain V_{DD}, and for which the chip can operate with a desired I_{SW}/I_{leak} ratio in the active mode and with $I_{subth}=I_{sub}$ in the standby mode. And this control system design is very useful in both active and standby modes to reduce any type of power consumption. And we will see all these in detail below sections.

4. MONITOR CIRCUITS

4.1 Delay Monitor

It is a combination of both the delay detector and V_{DD}/V_{th} Control switching block. And these are mainly used to control the delay based on the design in chip core.

4.1.1 Delay Detector

The Delay Detector is a circuit used to detect the relationship between clock cycle time and propagation delay in the chip core's critical path, controls the V_{DD} controller and the V_{DD}/V_{th} control switching block. And the delay detector circuit is shown in the below figure. The delay detector circuit consists of a critical path circuit, delay circuits (D), and registers. CLK is the clock signal of the internal circuits, CLK0 is a sampling clock for V_{DD}/V_{th} control, and Data is a one-shot pulse signal in a cycle of CLK synchronous CLK0s. D_{cp} and $D_{0\text{-}3}$ are comparator result signals, indicating differences between clock period T_{CLK} and various path delays that include, respectively, delay margins t_{cp} and $t_{0\text{-}3}$, where t_{cp} is delay in a critical path replica. If $t_* < T_{CLK}$ is true, D_* will be 1. Up, Down and Err are control signals used in V_{DD} control. If D_1=0, Up will be 1. If D_2=1, Down will be 1.

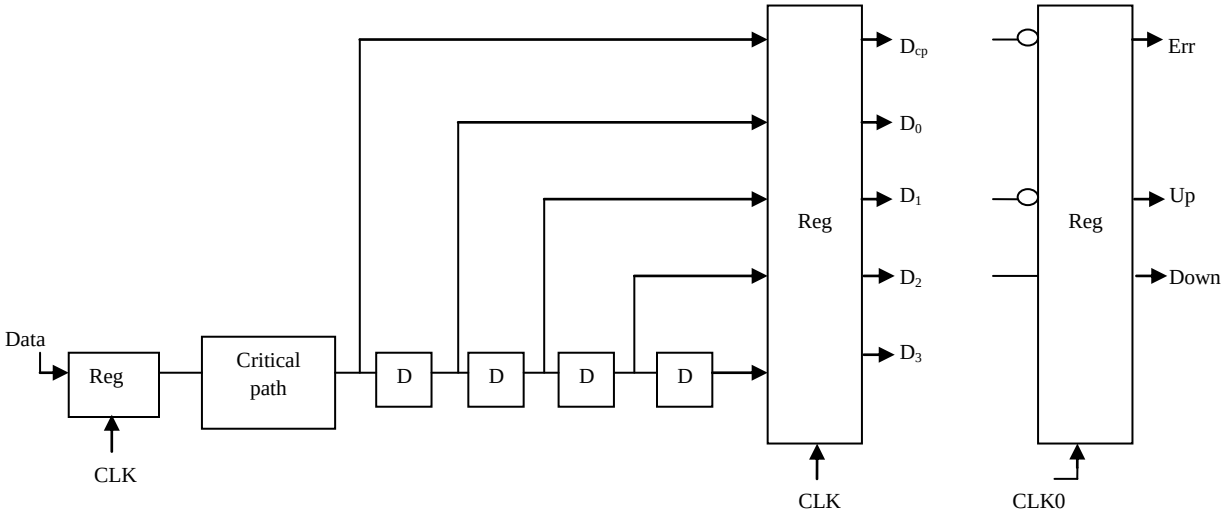

Figure 4: The Delay detector circuit.

4.1.2 V_{DD}/V_{th} control switching block

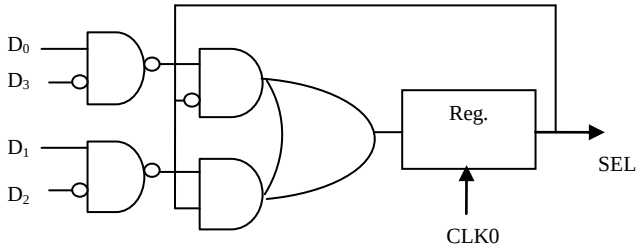

Figure 5: The V_{dd}/V_{th} control switching block.

As the name indicates, the V_{dd}/V_{th} control selection block selects either V_{dd} control or V_{th} control. SEL is the V_{dd}/V_{th} control selection signal. If SEL=1 represents the V_{dd} control mode and SEL=0 indicates the V_{th} control mode to avoid any oscillation problems. Figure 5. gives the architecture of V_{dd}/V_{th} control selection block. In V_{DD} control SEL(-1)=1, where SEL(-1) indicates the previous state, if $(D_1\ D_2)=(10)$, $t_1 < T_{CLK} < t_2$ is true, V_{DD} control will stop and V_{th} control will start. SEL(0)=0, where SEL(0) indicates the current state. In V_{th} control (SEL(-1)=0), if D_0=0 or D_3=1, $T_{CLK} < t_0$ or $t_3 < T_{CLK}$ is true, V_{th} control will stop and V_{DD} control will start. The table 1 indicates the truth table of V_{dd}/V_{th} control selection block and which explains all the operations involved in both the blocks.

Table 1: Truth table of V_{dd}/V_{th} control switching block.

Sel(-1)	D_{cp}	D_0	D_1	D_2	D_3	Sel(0)	Operations
V_{th} control	0	0	0	0	0	1	V_{dd} up err
	1	0	0	0	0	1	V_{dd} up
Sel(-1)=0	1	1	0	0	0	0	V_{th} control
	1	1	1	0	0	0	V_{th} control
	1	1	1	1	0	0	V_{th} control
	1	1	1	1	1	1	V_{dd} down
V_{dd} control	0	0	0	0	0	1	V_{dd} up err
	1	0	0	0	0	1	V_{dd} up
Sel(-1)=1	1	1	0	0	0	1	V_{dd} up
	1	1	1	0	0	0	V_{th} control
	1	1	1	1	0	1	V_{dd} down
	1	1	1	1	1	1	V_{dd} down

4.2 Active Power Monitor

The power monitor, a circuit for monitoring minimum chip power consumption, controls the V_{th} controller. It mainly involves 2 parts such as I_{SW} Monitor, I_{SW}-I_{leak} Comparator. And these are explained below.

4.2.1 I_{SW} Monitor

The I_{SW} monitor is a key component of power monitor. In V_{th} control, the I_{SW} monitor quickly generates a reference current I_{SW}' proportional to both clock frequency and supply voltage. When CLK=1, pre-discharge nMOSFETs discharge dynamic nodes and V_A and V_B. When CLK changes from 1 to 0, V_A and V_B increase with the flow of $1/\alpha.I_{sw}$' and $\alpha.I_{sw}$', where $0<\alpha<1$ and the value of α determines the precision of I_{SW}'.

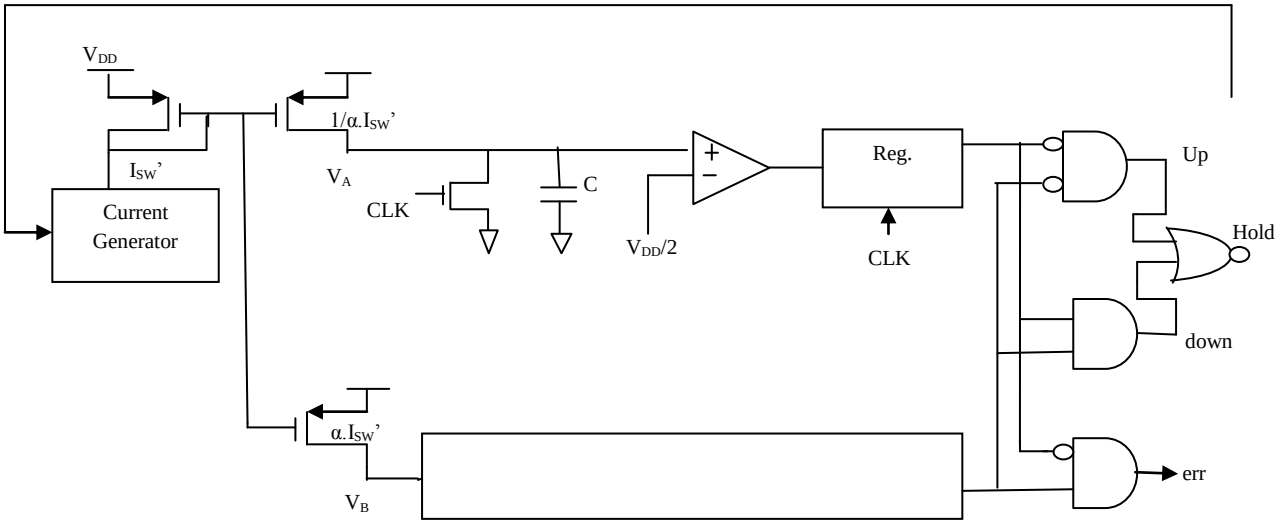

Figure 5: The I_{SW} Monitor circuit.

The outputs of the comparators, which detect $V_{DD}/2$ levels, are latched at rise clock edges. I_{SW} may be expressed as

$$I_{sw}=C.V_{DD}/2.2f=C.V_{DD}.f \qquad (7)$$

4.2.2 I_{SW}-I_{leak} Comparator

The I_{SW}-I_{leak} comparator then compares the I_{leak} values of leakage current replicas with I_{SW}', and the V_{th} control circuit adjusts body biases V_{NW} and V_{PW} on the basis of the comparison results. The results it produces are used to control body biases (V_{NW} and V_{PW}) so that leakage current will be maintained within the range of $\beta.I_{SW}$' to $1/\beta.I_{SW}$', where $0<\beta<1$. Majority-decision circuits are employed so as to avoid any problems resulting from abnormal leakage current due to device defects. $V_{PW}(V_{NW})$ is controlled in the range between RBB and FBB If $I_{leak}<I_{SW}$' is true, FBB_PW (FBB_NW) will be 1 and $V_{PW}(V_{NW})$ will change in the direction of FBB. If $I_{leak}>I_{SW}$' is true, RBB_PW (RBB_NW) will be 1 and $V_{PW}(V_{NW})$ will change in the direction of RBB. V_{th} control affects not only leakage current but also circuit delay. If $t_0< T_{CLK}< t_3$, which is a maximum permissible condition, is not true, V_{DD} control will start immediately and guarantee $t_{cp}< T_{CLK}$. And the architecture is shown in the following figure 6.

4.2.3 Standby Power Monitor

In the standby mode, the V_{th} controller increases V_{th} by adjusting V_{PW} and V_{NW} in the RBB direction, so as to reduce sub-threshold leakage current I_{subth}. When the optimum body bias is detected, V_{NW} and V_{PW} adjustment is stopped to avoid excessive reverse body bias. Fig.11 illustrates this circuit, which is an I_{subth}-I_{sub} comparator circuit for nMOSFETs.

Table 2: Truth table of Current Generator.

V_A	V_B	Operations
0	0	Isw' Up
0	1	Prohibition
1	0	Isw' Hold
1	1	Isw' Down

4.2.3.1 I_{subth}-I_{sub} comparator

It compares half the drain current of the left-side nMOSFET with the drain current of a right-side nMOSFET, and also compares the $(I_{subth}/2\text{-}I'_{subth}\text{-}I_{dg}/2)to(I_{gidl}/2)$. Where I'_{subth} is the right side nMOSFET of sub-threshold current, I_{DG} is drain-to-gate leakage current. There are three problems with this circuit: First, operation of the current mirror produces in a drop in drain voltage (V_{drain}), which results in erroneous values for I_{subth} and I_{sub}. Second, both I'_{subth} and I_{DG} are included in the value calculated for I_{subth} which makes it erroneous. And third, the value for I_{sub} becomes erroneous because I_{GB} is ignored in this calculation. And the architecture is shown the following figure 7. And the above problems can be overcome by the modified architecture and is shown the below figure 8. And which gives more precision than the normal comparator and reduced the voltage drop much.

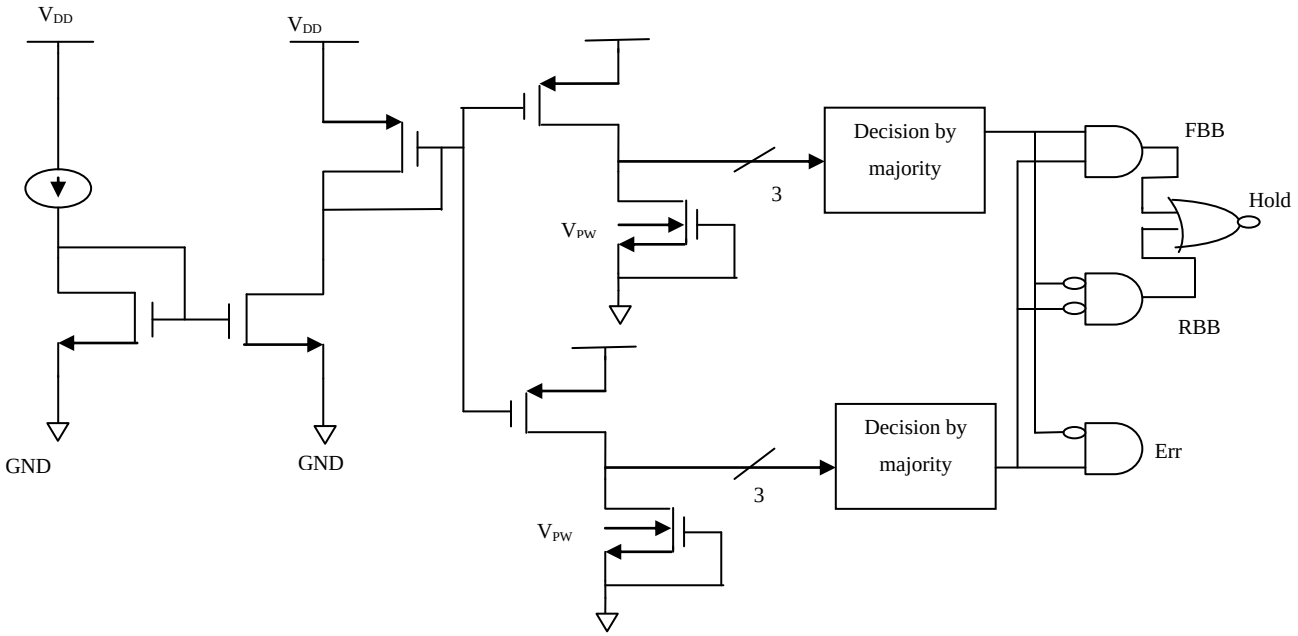

Figure 6: The I_{SW}-I_{LEAK} Comparator circuit.

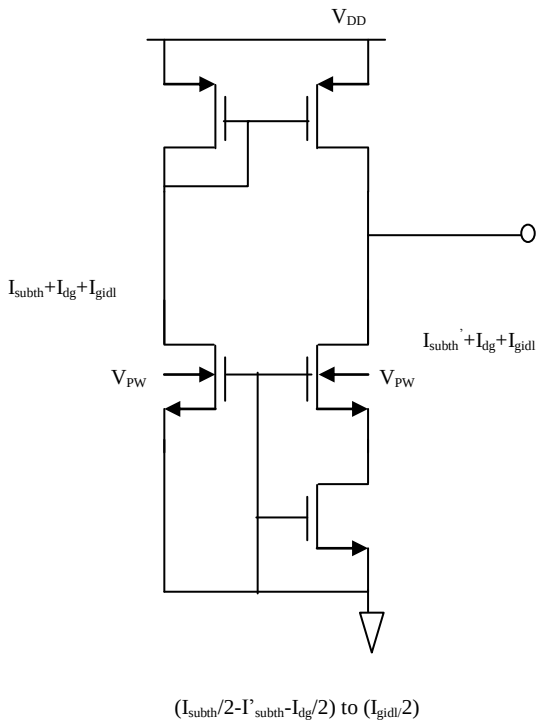

Figure 7: The I_{Subth}-I_{sub} Comparator circuit.

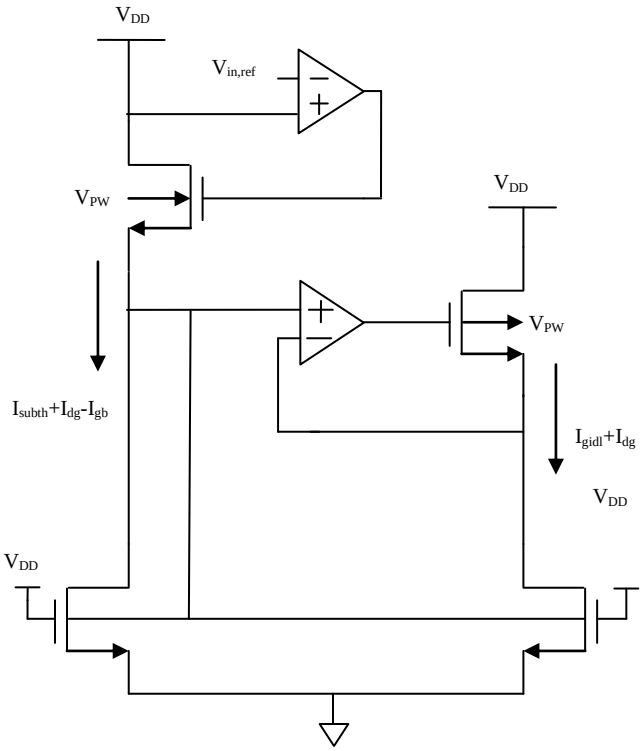

Figure 8: The modified I_{Subth}-I_{sub} Comparator circuit.

Our modified I_{Subth}-I_{sub} comparator circuit for optimum body bias monitoring of nMOSFETs. And it has overcome the above mentioned problems such as the reduction of voltage drop. In it, in order to achieve optimum body bias, we have taken into consideration the effects of lowering V_{DD} values and the effects of the presence of gate-oxide leakage. It maintains the V_{drain} of V_{DD}, monitors the source current (not the drain current of its left-side nMOSFET), and floats the source terminal for its right-side nMOSFET. The difference between the left nMOSFET's source current ($I_{subth}+I_{DG}-I_{GB}$) and the right nMOSFET's drain current ($I_{GIDL}+I_{DG}$) serves as a monitor of I_{subth} versus I_{sub}, which equals ($I_{GIDL}+I_{GB}$).

5. MEASUREMENT RESULTS

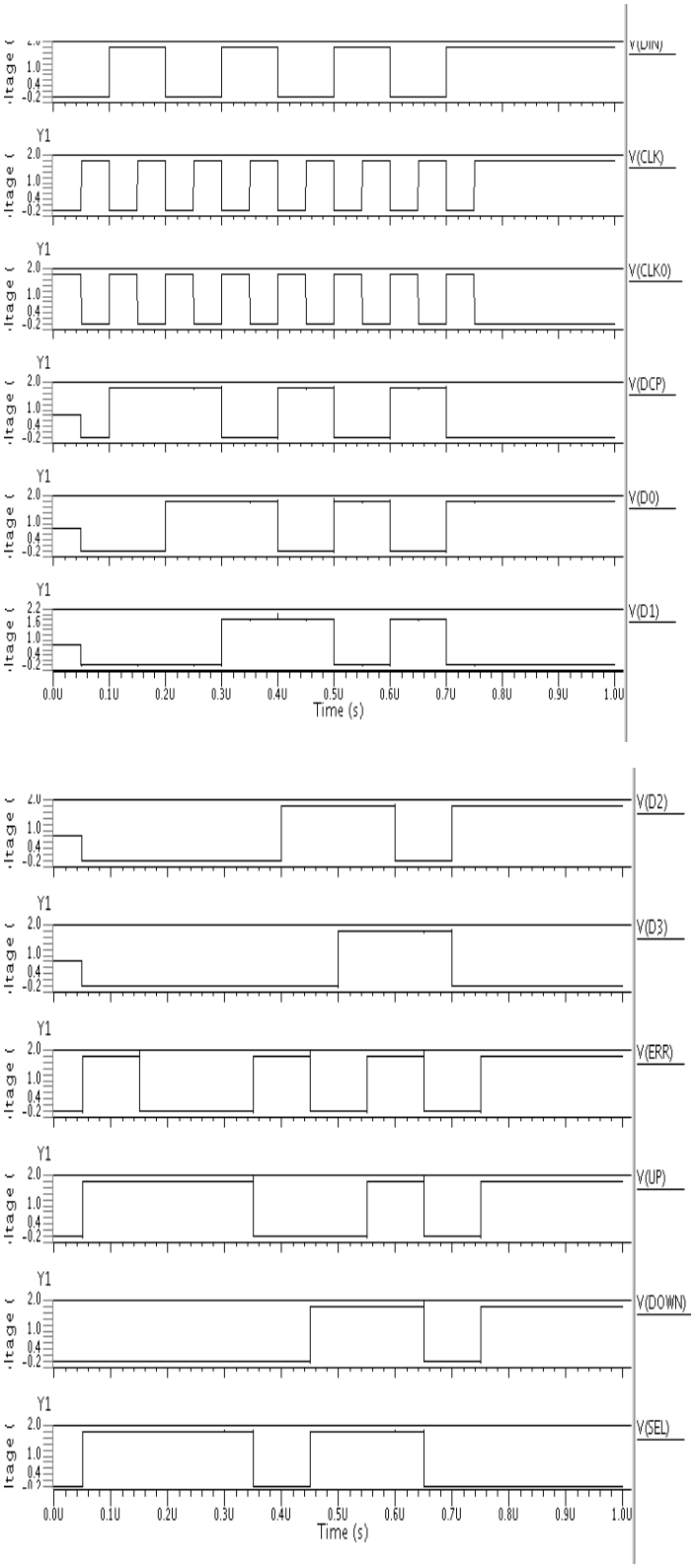

Figure 9: The Results of Delay monitor.

Table 3: The Leakage power consumption of all blocks.

Module name	Leakage current	Leakage power
Delay Detector	61.3nA	0.101uW
V_{DD}/V_{th} control block	18.1nA	0.032uW
V_{DD} control circuit	150.4nA	0.272uW
V_{th} control circuit	250.8pA	0.451nW
I_{sw} monitor	277.6nA	0.499uW
I_{sw}-I_{leak} comparator	135.2pA	0.243nW
I_{subth}-I_{sub} comparator	182.7nA	0.328uW
Modified I_{subth}-I_{sub}	217.6nA	0.391uW

Table 4: The Total Power consumption of all blocks.

Module name	Power consumption
Delay Detector	1.775uW
V_{DD}/V_{th} control switching block	0.37uW
V_{DD} control circuit	4.47mW
V_{th} control circuit	1.022nW
I_{sw} monitor	6.12mW
I_{sw}-I_{leak} comparator	3.45uW
I_{subth}-I_{sub} comprator	5.96mW
Modified I_{subth}-I_{sub}	5.43mW

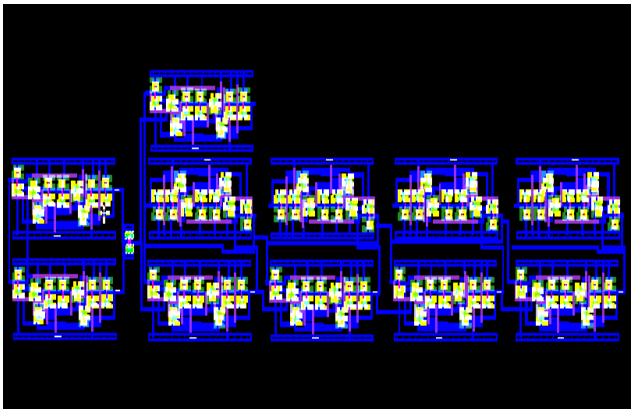

Figure 10: The implemented Layout of Delay Detector.

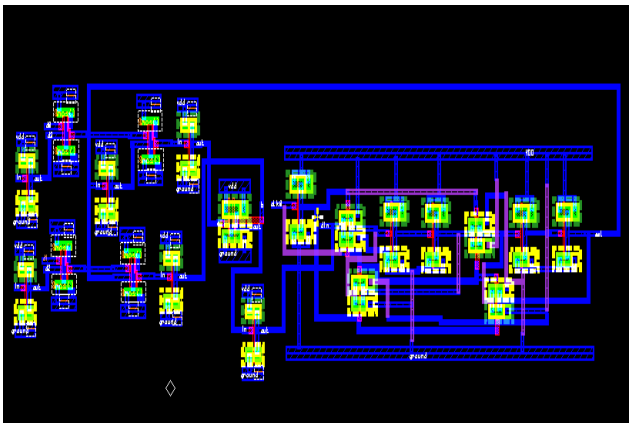

Figure 11: The implemented Layout of V_{dd}/V_{th} control block.

6. CONCLUSION

We have implemented both the Delay and Power monitoring schemes to reduce the power consumption. After completion of these schemes, during the layout construction (LVS) of delay monitor the power has been reduced (known by post layout simulation). The main challenge of schemes is the designing of comparator with a reduction of voltage drop. Though it may have some challenges, the power schemes are very useful for the reduction of leakage power, which plays an important factor in total power dissipation. Finally, we can say that the total power consumption has been efficiently reduced by 18%. And these schemes are very useful to reduce any type of leakage power in both active and standby modes.

7. ACKNOWLEDGEMENTS

The authors would like to thank their parents for their support and P. Magesh Kannan for his valuable suggestions and advice.

8. REFERENCES

[1] Masahiro Nomura, Yoshifumi Ikenaga, Koichi Takeda, yoetsu Nakazawa, "Delay and power monitoring schemes for minimizing power consumption by means of supply and threshold Voltage control in active and standby modes", in IEEE Journal of solid state circuits, vol.41, Apr.2006, pp. 805-814.

[2] V. R. von Kaenel, M. D. Pardoen, E. Dijkstra, and E. A. Vittoz, "Automatic adjustment of threshold and supply voltages for minimum power consumption in CMOS digital circuits," in IEEE Symp. Low Power Electronics Dig. Tech. Papers, Oct. 1994, pp. 78–79.

[3] J. T. Kao, M. Miyazaki, and A. P. Chandrakasan, "A 175-mV multiply accumulate unit using an adaptive supply voltage and body bias architecture," IEEE J. Solid-State Circuits, vol. 37, no. 11, pp. 1545–1554, Nov. 2002.

[4] K. Nose and T. Sakurai, "Optimization of V_{DD} and V_{TH} for low power and high-speed applications," Proc. ASP-DAC, pp. 469–474, Jan. 2000.

[5] T. Kuroda, K. Suzuki, S. Mita, T. Fujita, F. Yamane, F. Sano, A. Chiba, "Variable supply volt zoltage scheme for low power high speed CMOS digital design," IEEE J. of solid state Circuits, vol.33,pp.454-462, Mar.2003.

[6] C. Neau and K. Roy, "Optimal body bias selection for leakage improvement and process compensation over different technology generations," in Proc. IEEE Int. Symp. Low Power Electronics and Design (ISLPED), Aug. 2003, pp. 116–121.

[7] M. Nakai, S. Akui, K. Seno, T. Meguro, T. Seki, T. Kondo, A. Hashiguchi, H. Kuwahara, K. Kumano, and M. Shimura, "Dynamic voltage and frequency management for a low-power embedded microprocessor," IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 28–35, Jan. 2005.

[8] M. Nomura, Y. Ikenaga, K. Takeda, , Y. Aimoto, and Y. Hagihara, "Monitoring scheme for minimizing power consumption by means of supply and threshold voltage control in active and standby modes," in Symp. VLSI Circuits Dig. Tech. Papers, Jun. 2005, pp. 308–311.

[9] R. Kumar, C.P. Ravikumar, "Leakage power estimation for deep submicron circuits in an ASIC design environment", Design Automation Conference on VLSI Design, ASP-DAC 2002, 7-1 1 Jan. 2002, pp. 45 - 50.

[10] K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-sub micrometer CMOS circuits", IEEE, Vol. 91, No. 2, Feb. 2003, pp. 305 - 327.

[11] O. Semenov, A. Pradzynski, M. Sachdev, "Impact of gate induced drain leakage on overall leakage of submicrometer CMOS VLSI circuits", IEEE Transactions on Semiconductor Manufacturing, Vol. 15, No. 1, Feb. 2002, pp. 9 - 18.

Pavan K Tadavarthi was born in Narasaraopet, Andhra Pradesh, India on May 15, 1988. He received his Bachelor of Technology degree in Electronics & Instrumentation Engineering (E.I.E.) from S.V.E.C, Tirupathi which is affiliated to J.N.T.University, Ananthapur, A.P. in the year 2009. Currently he completed his M.Tech. Programme in VLSI Design from VIT University, Vellore, Tamil Nadu in the year 2011. His areas of interest are Digital IC Design, ASIC Design and Low power IC Design. And Mr. T.K. Pavan is a member of the Instrumentation Society of India (ISOI) student chapter.

Nagaraju Vutukuri was born in Narasaraopet, Andhra Pradesh, India on March 08, 1987. He received his Bachelor of Technology degree in Instrumentation & Control Engineering (I.C.E.) from N.E.C, Narasaraopet which is affiliated to J.N.T.University, A.P. in the year 2008. Currently he completed his M.Tech. Programme in Communication Engineering from VIT University, Vellore, Tamil Nadu in the year 2011. His areas of interest are Digital IC Design and Digital Communications.