Fully Robust Path Delay Fault Testability using KEP-SOP

G. P. Sinsinwar
Associate Professor
Govt. Engineering College
Bikaner (Rajasthan) India

K.S.Yadav
Professor
Northern India Engineering College, Delhi (India)

Abhishek Acharya
Assistant Professor
Govt. Engineering College
Bikaner (Rajasthan) India

ABSTRACT
Full testability is a desirable property network and maintaining the testability of multi-level logic synthesis is very complicated. In our paper propose new technique which maintains fully testable circuit with function mode under the robust path delay fault model. The preservation of testability of these networks under the stuck-at-fault model and Path delay model, preservation of testability the K-EPSOP is typical but it we proposed robust path delay fault model using binate property of variable with mux realization for remainder or without remainder. The whole our new architecture gives guarantees the path delay fault fully testable circuit a modification in design and operates on mode e.g. functional mode.

Key Words: **Design for testability, logic synthesis, multiplexor-based circuits, K -EPSOP.**

1. INTRODUCTION
The SOP minimization synthesis is easy with small number of level using very efficient heuristic for logic minimization ESPRESSO (2), SCG (4) and approximation algorithms for fully testable KEP-SOP network available. Multi-level minimization Unbounded multilevel minimization algorithms SIS (3) and BDD Based circuit (4, 9) are very fast and the resulting network is often compact. Bounded multi level EXSOP (7), OR-AND-OR (8), SPP (9) &EPSOP(8&1)and the bound promising for high quality but huge minimization time required for their synthesis. KEP-SOP form minimization, an approximation algorithm which guarantee near optimum solution with polynomial time and utilize the projection of SOP form into subspaces of Boolean space that reduces the hamming distance among the cube appearing in each subspaces(1). BDD based optimization for Path Delay Fault Testability (10).Testability of KEP-SOP networks under the stuck-at-fault(11) uses Mux is 100% testable but the some network is not delay fault testable under the robust path delay model because the multiplexer will destroyed the testability of the network. In our new approach will maintain the robust delay fault testability and whole design work on Functional mode with one control signals.In Section 2, the delay fault testability of network which explain the K-EPSOP form realization and projections of Boolean terms into the different spaces [1] and its implications on testability preservation. The pdf testability property using mux[11], BDD optimization[10],multi-valued minimization with PLA & output EXOR gate[5] and BDD based synthesis of symmetric circuit[9]. In Sections 2.B, we study the testability preservation of the K-EPSOP form path delay fault using muxes realization with remainder or without remainder. The whole architecture gives guarantees the path delay fault testable circuit. In Section 3, we provide experimental results and suggest a modification in design that proved our new architecture is fully testable and operates on both the modes e.g. functional and test mode. Finally, conclusions are given in Section 4

2. PRELIMINARIES
Let f : $\{0, 1\}^n \rightarrow \{0, 1\}$ a Boolean function which is having n variables $x_1, x_2 \ldots x_n$ and basis on the characteristics of function partitioned into two disjoint subspace, with couple of variables e.g. x_i and x_j . One is $(x_i \oplus x_j)$ when $x_i \neq x_j$ and $(x_i \oplus x_{j'})$ when $x_i = x_j$ where i < j.The total funtion f as the summation f two projections of Φ, $\Phi_{\oplus}, \Phi_{\oplus}^{-}$ into the two subspaces $\Psi i,j = (x_i \oplus x_j)\Phi_{\oplus} + (x_i \oplus x_j')\Phi_{\oplus}^{-}$.

Remaining terms of Boolean function which are not projected into two subspaces. Again search another couple of variables to create more subspace. If another couples of variables are not suitable to create more subspace. So unprojected SOP terms is called remainder.

RSOP $\Psi i',j'(x_i' \oplus xj')\ \rho_{\oplus} + (x_i \oplus \overline{xj}')\ \rho_{\oplus}^{-}$

The expression $\Psi i,j$ is called the (i, j)-EP-SOP of function. Previous paper shows the design is stuck-at-fault testable but it is not path delay testable circuit which is shown in figure 2(a) without remainder and figure 2(b) with remainder. This network said to be stuck-at-fault 100% testable basis on the node property. If each node of circuit C does not have redundancy fault hence node is testable or network is testable.

2. A PATH DELAY FAULT TESTABILITY OF KEP-SOP FORM

In realization of BDD using the MUX cells connected to constant values, will "destroys" the testability. The stuck-at-fault Model (SAFM) doesn't ensured the100% testability of EP-SOP with and without remainder by adding fix number of extra inputs mux and gate. A path delay fault model consist path of sequence of i gates $\{g_o, g_1, \ldots, g_n, g_{n+1}\}$.*Each gate having two inputs, off-inputs/side inputs and on-input. Under robust path delay fault model, one input of gate is non-controllable which is used for propagation of transient from input to output. For example, 1 is the non-controllable of AND gate and 0 is non-controllable for OR gate.*

The propagation delays of all paths are less than the system clock interval. A transition having a pair of patterns (I1 (initialization vector), I2 (propagation vector)) is required, rather than a single pattern as in the SAFM. At each mux cell, the values 10 or 01 can be applied (dependent on t). Thus, the paths starting at an input corresponding to the variable xi can be propagated along any of the two AND-gates. Furthermore, due to the propagation along the Multiplexors, it is easy to see that the paths starting at t can be tested in Fig.-1

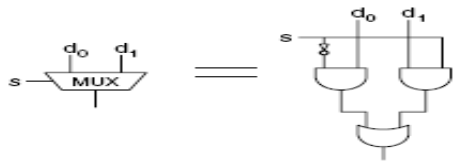

Figure 1: MUX Representation

Additional input and one inverter, a circuit can be generated from a BDD that is 100% testable for robust path-delay faults. But when the circuit can be generated EPSOP then circuit is 100% testable for robust path-delay faults by two additional for without remainder and three additional input for with remainder.

An arbitrary multiplexor circuit with the data inputs (d0, d1) at least one of the patterns P0=(0,1) or P1=(1,0) is applicable. The data inputs of a multiplexor imply full testability with respect to the PDFM two patterns for a robust test for path delay faults can be carried out in polynomial time. In our technique, replacement of AND Gates and OR gates by using muxes to make the network guarantee robust path delay fault 100 % testable and also limits the infinite number of path in network.

3. LOGIC SYNTHESIS 2EP-SOP WITH BINATE PROPERTY

Synthesis of any function is important with respect to testability with 2EP-SOP by using the binate property of the remaining variables those are not projected in any four spaces. We synthesize a Boolean function in following steps

Let Boolean function,

f = $\overline{x1}$ x2 $\overline{x3}$+ x1 $\overline{x2}$ $\overline{x3}$ + $\overline{x1}$ $\overline{x2}$ x3+ x1 x2 x3 x4 +$\overline{x4}$ x5 $\overline{x6}$ + x4 $\overline{x5}$ $\overline{x6}$ + $\overline{x4}$ $\overline{x5}$ x6 + x3 x5 $\overline{x6}$

Ex-OR form of above Boolean function with two couples of variables x1,x2 & x4,x5 and t=1 control variable will be

=(x1⊕x2)$\overline{x3}$ +(x1⊕$\overline{x2}$)($\overline{x2}$ $x3 + x3\ x4$)+(x4⊕x5) $\overline{x3}$ +(x4 ⊕$\overline{x5}$) ($\overline{x5}$ $x6 + x3\ x5$ $\overline{x6}$)

The projections based on one couple of variable 1EPSOP

$\zeta_{i,j}$ =(xi ⊕xj) $\Phi_{\oplus}$ +(xi⊕$\overline{xj}$) $\Phi_{\overline{\oplus}}$

The projections based on two couple of variable 2EPSOP

$\zeta_{i,j,i',j'}$==(xi⊕xj)$\Phi_{\oplus}$+(xi⊕$\overline{xj}$)$\Phi_{\overline{\oplus}}$+(xi'⊕xj')$\rho_{\oplus}$+(xi⊕ $\overline{xj'}$) $\rho_{\overline{\oplus}}$ projections

Overall is the sum of all projections

ζ =! $\Phi_{\oplus}$! + ! $\Phi_{\overline{\oplus}}$! + ! $\rho_{\overline{\oplus}}$! + ! $\rho_{\oplus}$!

In third step we search the variable which are presents in all four projected spaces and binate in behavour for in this example x3 variable ($\overline{x3}$ & x3) which is available in both form or binate in behavour in nature and also consider it as control variable. A single or group of variables those are not placed in any couples of variable that will be the remainder.

Synthesis by using BDD and realize using mux. Our new architecture figure 2(c) without remainder and figure 2(d) with remainder, robustly tested path delay fault model which is 100% testable because it work on functional mode with the help of some control signals (t=1). Two tests for each physical path have to carried for both rising or falling transitions. Our circuit works with the mode:

f(x1,x2….xn)at x3=0

= (x1⊕x2)+(x4⊕x5)+(x4 ⊕$\overline{x5}$)($\overline{x5}$x6)

f(x1,x2….xn)at x3=1

= (x1⊕ $\overline{x2}$) ($\overline{x2}$+x4) + (x4 ⊕$\overline{x5}$) ($\overline{x5}$x6 + x5$\overline{x6}$)

Functional mode:
t=1 RSOP - Remainder

SOP1=($\overline{x2}$+x4) Robustly-No delay fault

SOP2= ($\overline{x5}$x6 + x5$\overline{x6}$) Robustly -No delay fault

SOP3= ($\overline{x5}$ $x6$) Robustly --No delay fault

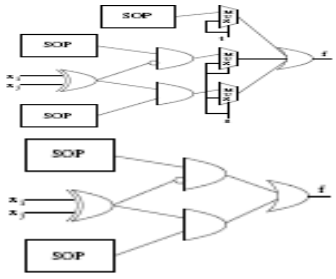

Figure 2 (a) With Remainder 2 (b) Without remainder

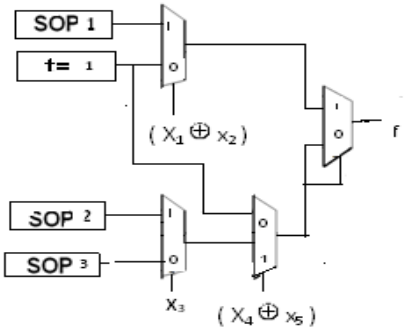

Figure2 (c) Without remainder

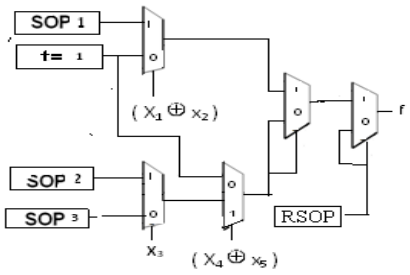

Figure 2 (d) with remainder

4. EXPERIMENTAL RESULTS

General multiplexor based network is directed acyclic along with any path from inputs to the circuit output. A multiplexor based network corresponding to a binary decision diagram of a given multilevel circuit satisfy the restriction that along any path from input to output the decision variable is encountered at most. The percentage of paths that can be covered by a RPDF test for these coverage large variations can be observed. The minimization of function by using BDD with respect to one criterion gives the least number of nodes when minimized with respect to paths using the heuristic minimization algorithms such that all functions are irredundant and each product term is prime at least one output followed by 1EP-SOP and 2EP-SOP factorization with both remainder or non-remainder. The technology mapping with multiplexor or AND-OR used the Design Complier (DC from Synopsys) and netlist generated .By using netlist the paths are generated. That comprises the sequences of gates .For each selected path generates the pattern using GA Based iterative algorithm such that each can able to transmit the input signal to output. Our approach includes a conventional delay test ATPG. The mapping of EP-SOP circuit using muxes for functional mode is 100% robustly testable. The algorithm was coded in C language on SIS system environment

5. CONCLUSIONS

The current robustly delay test technique focus only the whole realization using mux in the functional mode that achieve 100% testability of the 2EP-SOP circuits. It was shown that the reduction of the number of paths in the BDD can significantly reduce the number of test patterns needed to test the circuit with respect to the PDFM. An adjustable objective function was used to take more than one goal during synthesis into account and thereby to compromise e.g. between size and number of test patterns needed. The our approach show mux-circuits are synthesized with guaranteed 100% testable under the PDFM at the cost of one stable input t=1 no additional inputs are required.

6. REFERENCE

[1] A. Bernasconi.V. Ciriani R. Cordone" An Approximation Algorithm for Fully Testable kEP-SOP Networks" *GLSVLSI'07,* March 11–13, 2007

[2] R. Rudell and A. Sangiovanni-Vincentelli. Multiple-valued Minimization for PLA Optimization. IEEE Trans. on CAD, 6:727–750, 1987.

[3] E. M. Sentovich, K. Singh, L. Lavagno, C. Moon, A. S. R. Murgai, H. Savoj, P. Stephan, R. Brayton, and A. Sangiovanni-Vincentelli. SIS: A system for sequential circuit synthesis. Technical report, 1992.

[4] R. Drechsler, J. Shi, and G. Fey. Synthesis of Fully Testable Circuits from BDDs. IEEE Trans. on CAD of Integrated Circuits and Systems, 23(3):440–443, 2004

[5] D. Debnath and T. Sasao. Multiple–Valued Minimization to Optimize PLAs with Output EXOR Gates. In IEEE International Symposium on Multiple-Valued Logic, pages 99–104, 1999.

[6] D. Debnath and Z. Vranesic. A Fast Algorithm for OR-AND-OR Synthesis. IEEE Transactions on CAD, 22(9):1166–1176, 2003.

[7] F. Luccio and L. Pagli. On a New Boolean Function with Applications. IEEE Transactions on Computers, 48(3):296–310, 1999.

[8] R. Ishikawa, T. Hirayama, G. Koda, and K. Shimizu. New Three-Level Boolean Expression Based on EXOR Gates. IEICE Transactions on Information and Systems, (5):1214–1222, 2004.

[9] Junhao Shi Görschwin Fey Rolf Drechsler "BDD based Synthesis of Symmetric Functions with Full Path-Delay Fault Testability" Proceedings of the 12th Asian Test Symposium (ATS'03)

[10] Görschwin Fey Junhao Shi Rolf Drechsler"BDD Circuit Optimization for Path Delay Fault Testab Proceedings of the EUROMICRO Systems on Digital System Design (DSD'04)

[11] P. Ashar, S. Devadas, and K. Keutzer. Path-delay-fault testability properties of multiplexor-based networks. *INTEGRATION, the VLSI Jour.*, 15(1):1–23, 1993.