Reduction of Power Dissipation in Logic Circuits

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ABSTRACT
The most research on the power consumption of circuits has been concentrated on the switching power and the power dissipated by the leakage current has been relatively minor area. In today's IC design, one of the key challenges is the increase in power dissipation of the circuit which in turn shortens the service time of battery-powered electronics, reduces the long-term reliability of circuits due to temperature-induced accelerated device and interconnects aging processes, and increases the cooling and packaging costs of these circuits. In this paper the main aim is to reduce power dissipation. A new design method for various logical circuits design, which is low power, compared to general Static CMOS logic. In this technique both NMOS transistor and PMOS transistors in various logic circuits is split into two transistors. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor Leakage current flowing through the PMOS transistor stack reduces due to the increase in the source to substrate voltage in the top PMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor. The tool used is TANNER EDA for schematic simulation. The simulation technology used is MOSIS 180nm.

Keywords: Stack, 6T SRAM cell, low power, threshold voltage.

1. INTRODUCTION

In recent years, power consumption has become a critical design concern for many VLSI systems. Historically, one of the advantages of complementary metal-oxide-semiconductor (CMOS) over competing technologies [1], such as transistor-transistor logic (TTL) and emitter coupled logic (ECL), has been its lower power dissipation [8]. When not switching, CMOS transistors have, in the past, dissipated negligible amounts of power. But now the scenario has been changed, current leaks in the transistors even when they are not switching [7].

In next generation technologies leakage power [2][9] is expected to be more significant as threshold voltage decreases in conjunction with supply voltage as technology scales and due to sizing of transistors [14]. Even in current-generation technology, sub threshold leakage power dissipation is comparable to the dynamic power dissipation, and the fraction of the leakage power will increase significantly in the near future. Today's microprocessor designs devote a large fraction of the chip area [5] to the memory structures. High-performance on-chip caches are a crucial component in the memory hierarchy of modern computing systems.In this technique each NMOS and PMOS transistors in the logic gates is split into two transistors as shown in Fig 1 and so called Stack Technique [10]. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor. This reduces the power dissipation in logic circuits. This technique is implemented to BASIC gates such as AND,OR,XOR etc ,COMBINATIONAL circuits such as FULLADDER, SEQUENTIAL circuits such as D-Flip-flop and also for memory cells such as 6TSRAM CELL.

2. IMPLEMENTATION IN LOGIC GATES
The proposed technique is implemented to the CMOS LOGIC GATES such as INVERTER, AND, NAND, NOR, XOR etc.

2.1 CMOS Inverter
Shown an inverter circuit, when the input to circuit is a ground voltage the PMOS transistor is turned ON while both the NMOS transistors are turned OFF. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor[4].This technique introduce considerable performance overhead due to stacking of transistors[11]. Implementation of stack technique is shown in fig 1 which leads to low leakage power [12]. The schematic of inverter is shown in fig 2.

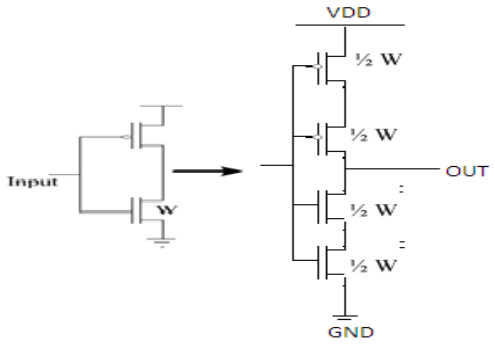


Fig 1 CMOS Inverter Stack Technique

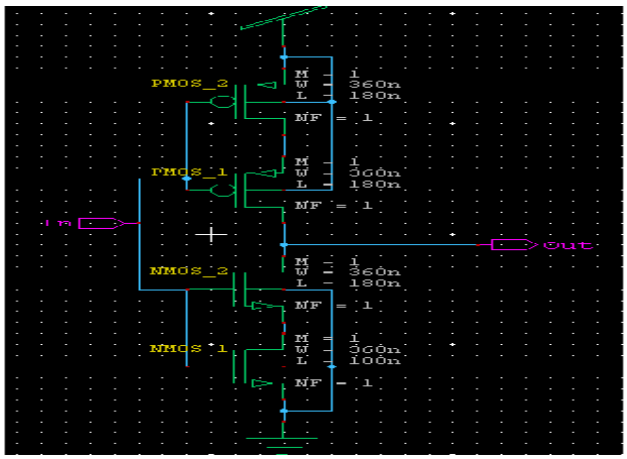
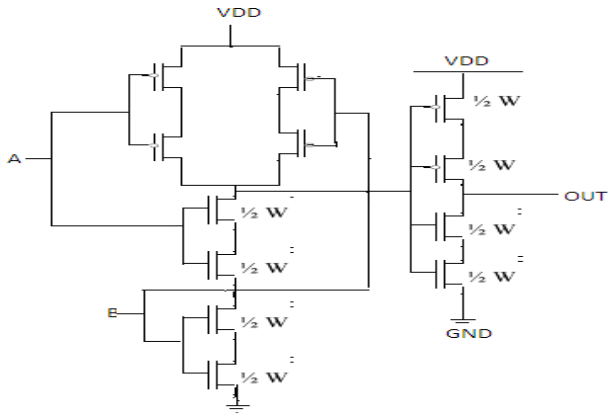


FIG 2: CMOS INVERTER SCHEMATIC

2.2 AND GATE:

The proposed technique is implemented for AND gate where both NMOS and PMOS transistors split in to two transistors as shown in fig 3. . Implementation of stack technique is shown in fig 3 and respective schematic is shown in fig 4



. FIG 3 CMOS AND STACK TECHNIQUE

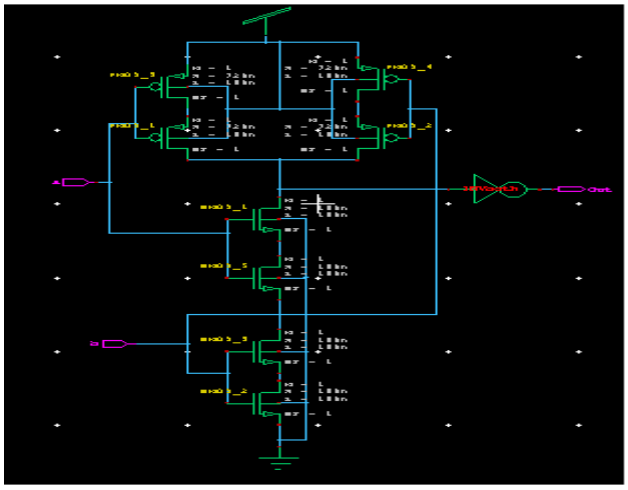


FIG 4 CMOS AND SCHEMATIC

2.3 OR GATE:

The proposed technique is implemented for OR gate where both NMOS and PMOS transistors split in to two transistors as shown in fig 6. . Implementation of stack technique is shown in fig 6 and respective schematic is shown in fig 7.

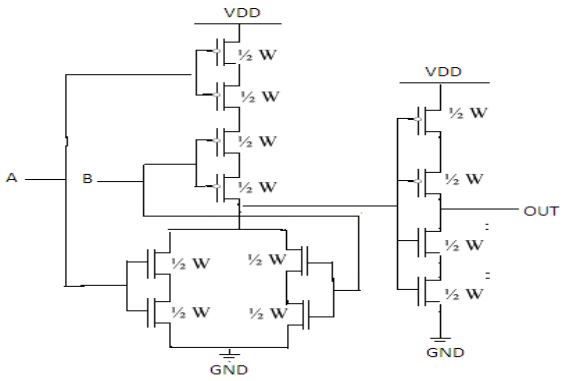


FIG 5 CMOS OR STACK TECHNIQUE

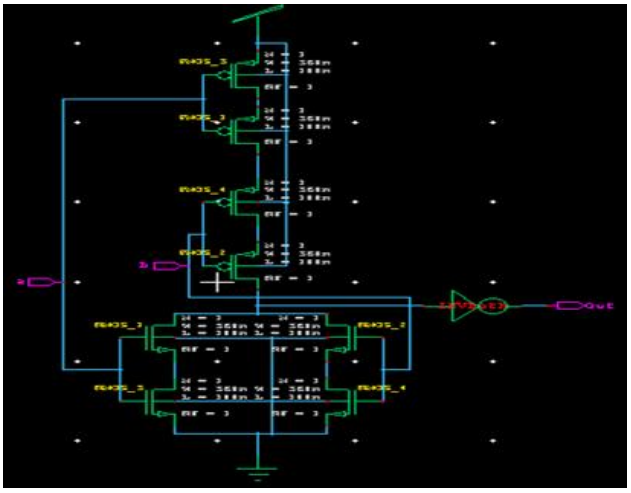
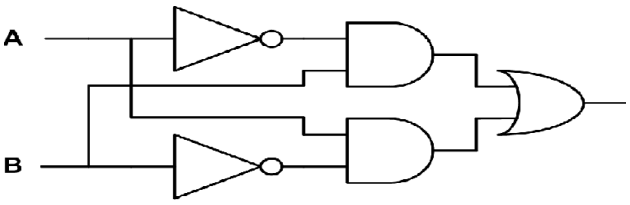


FIG 6 CMOS OR SCHEMATIC

2.4 XOR GATE:

The proposed technique is implemented for XOR gate using NAND, OR, INVERTER where both NMOS and PMOS transistors split in to two transistors in each of the respective gates. Basic XOR gate is shown in fig 7 and respective schematic is shown in fig 8



A xor B = A'B + AB'

FIG 7 BASIC XOR GATE

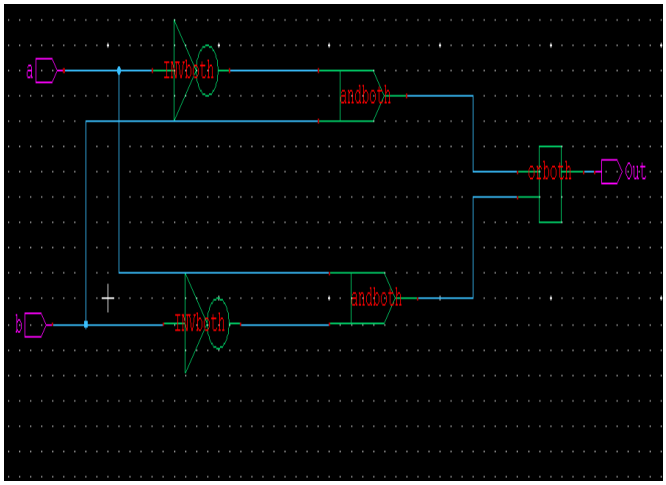


FIG 8 CMOS XOR SCHEMATIC

3. IMPLEMENTATION IN COMBINATIONAL CIRCUITS

In digital circuit theory, combinational logic (sometimes also referred to as combinatorial logic) is a type of digital logic which is implemented by Boolean circuits, where the output is a pure function of the present input only. Combinational logic is used in computer circuits to do this Boolean algebra on input signals and on stored data. Practical computer circuits normally contain a mixture of combinational and sequential logic. For example, the part of an arithmetic logic unit, or ALU, that does mathematical calculations is constructed using combinational logic. Other circuits used in computers, such as half adders, full adders, half subtractors, full subtractors, multiplexers, demultiplexers, encoders and decoders are also made by using combinational logic.

3.1 FULL ADDER

To construct a full adder circuit, we'll need three inputs and two outputs. Since we'll have both an input carry and an output carry, we'll designate them as C_{IN} and C_{OUT}. At the same time, we'll use S to designate the final Sum output. The design of Full Adder using XOR, AND, OR is shown in Fig.9.The stack technique [13] is implemented for this full adder and the schematic is shown in fig 10.

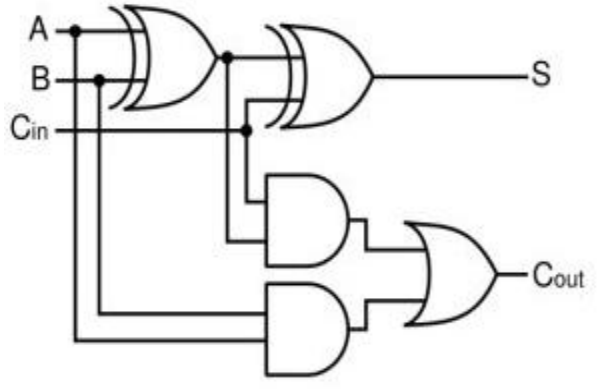


FIG 9 FULL ADDER CIRCUIT

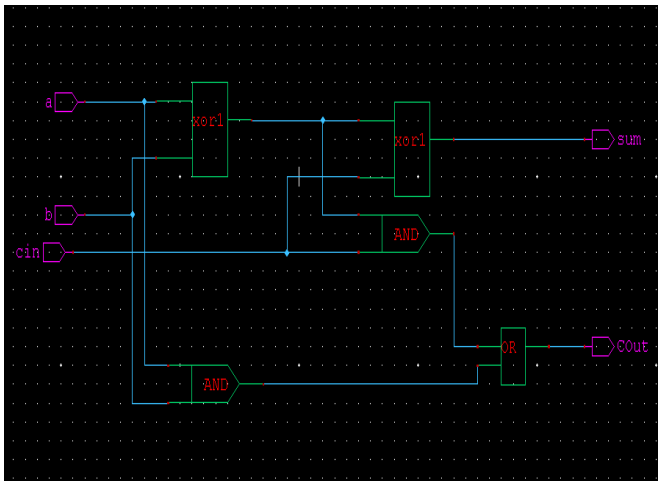


FIG 10 FULLADDER SCHEMATIC

4. SEQUENTIALCIRCUITS

Sequential circuit is one that has a memory element involved with it. Now take any flop, data is latched by the flop on the active edge of the clock, so data is held in the flop till the next active edge of the clock. So the flop acts as a memory element where data is held for a certain period of time based on your clockperiod.This is same for d flop**.**

4.1 D-FLIP FLOP

The D flip-flop shown in Figure 11 is a modification of the clocked SR flip-flop. The D input goes directly into the S input and the complement of the D input goes to the R input. The D input is sampled during the occurrence of a clock pulse. If it is 1, the flip-flop is switched to the set state (unless it was already set). If it is 0, the flip-flop switches to the clear state. The D-Flip-flop using NAND and NOT gate is shown in fig 11 and respective schematic with implementation of stack technique is shown in fig 12

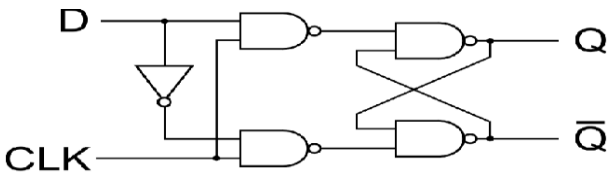


FIG 11 D-FLIP-FLOP CIRCUIT

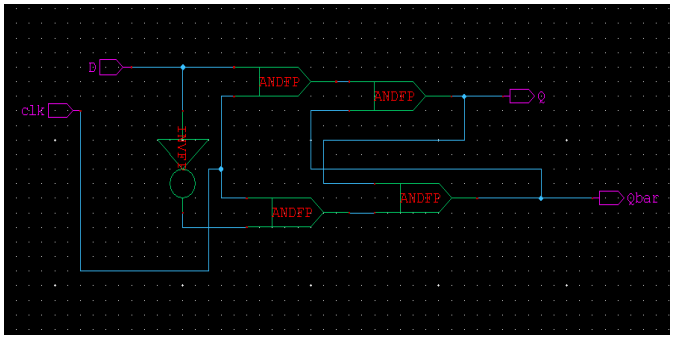


FIG 12 D-FLIP-FLOP SCHEMATIC

5. MEMORY CELL STRUCTURES

5.1 SRAM CELL STRUCTURE

The mainstream six-transistor (6T) CMOS SRAM cell is shown in Fig 13. Similarly to one of the implementations of an SR latch, it consists of six transistors. Four transistors (*M*1-*M*4) comprise cross-coupled CMOS inverters and two NMOS transistors *M*5 and *M*6 provide read and write access to the cell. Upon the activation of the word line, the access transistors connect the two internal nodes of the cell to the true (BL) and the complementary (BLB) bit lines. A 6T CMOS SRAM cell is the most popular SRAM cell [6] due to its superior robustness, low power and low-voltage operation. The schematic of 6T SRAM cell shown in Figure 14 consists of a Sense Amplifier and a precharge circuit. The primary function of a Sense Amplifier in SRAM cells is to amplify a small analog differential voltage developed on the bit lines by a read-accessed cell to the full swing digital output signal thus greatly reducing the time required for a read operation. A Sense Amplifier allows the storage cells to be small, since each individual cell need not fully discharge the bit line. A precharge circuit is used in order to drive the supply voltage. An SRAM cell must be designed such that it provides a non-destructive read operation and a reliable write operation. Implementation of stack technique shown in fig 13 reduces power dissipation. Reduction in the leakage power [3] of even a single cell of cache can on the whole reduce a large fraction of the total power chip caches. The respective schematic is shown in fig 14.

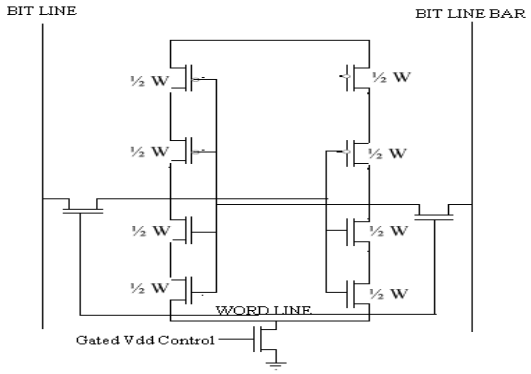


FIG 13 SRAM STACK TECHNIQUES

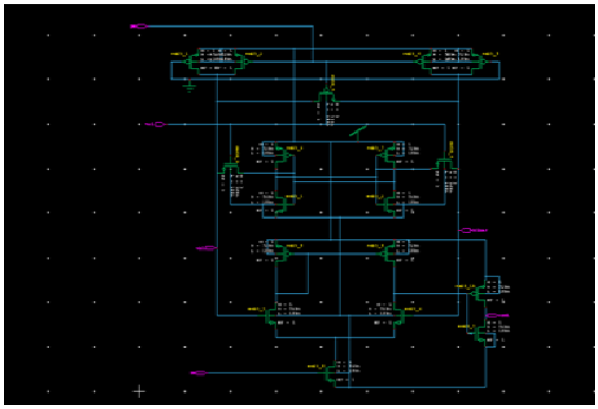


FIG 14 SCHEMATIC OF 6T SRAM CELL

6. WAVEFORMS

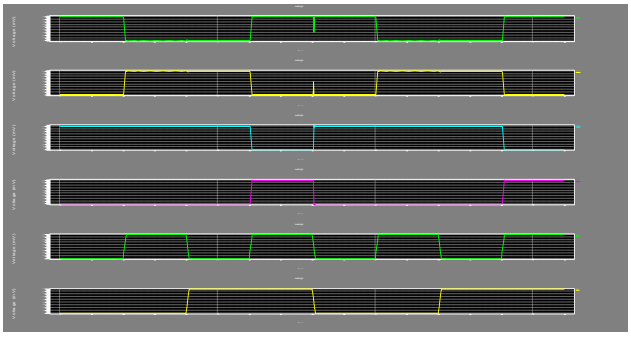


FIG 15 CMOS LOGIC GATES

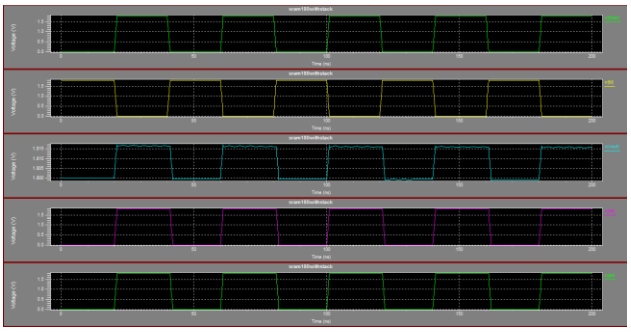


FIG 16 WAVEFORM FOR 6T SRAM CELL

6. PRACTICAL OBSERVATIONS

Table 1 Power dissipations in basic gates

S.No	Basic gates	Conventional (µw)	With stack (µw)
1	Inverter	1.8192µw	0.7613
2	And	2.3224µw	1.3481
3	Nor	1.2645µw	0.8334
4	Xor	5.8675 µw	2.6845

Table 2 Power dissipations in combinational, sequential and memory cell structure

S.No	Circuits	Conventional (µw)	With stack (µw)
1	Full adder	2.9242	1.8924
2	D-flip-flop	5.6690	5.1954
3	6T SRAM	0.32524	6.3212

8. CONCLUSION

Implementing the STACK technique can reduce power dissipation of the LOGIC CIRCUITS. We can observe the reduction in power dissipation from Conventional to the Proposed Stack Technique in combinational, sequential as well as in memory cell structures. The tool for simulation is TANNER and at 180 nm technology and the practical observations has been tabled.

9. REFERENCES

[1] 2007 International Technology Roadmap for Semiconductors, [online]. Available http://public.itrs.net.

[2]. J.Abraham, "Overcoming timing, power bottlenecks," EE Times, April 2003.

[3]. P. Elakkumanan, C. Thondapu, and R. Sridhar, "A Gate Leakage Reduction Strategy for Sub-70nm Memory Circuit," in Proceedings of 2004 IEEE Dallas/CAS Workshop, 2004, pp. 145-148.

[4]. Z. Chen, M. Johnson, L. Wei and K. Roy, 'Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modelling of Transistor Stacks,' *International Symposium on low Power Electronics and Design*, pp. 239-244, August 1998.

[5]. S. Dutta, S. Nag, K. Roy, "ASAP: A Transistor Sizing tool for speed, area, and power optimization of static CMOS circuits", *IEEE International Symposium on Circuits and Systems*, pp. 61-64, June, 1994

[6]. N. Azizi and F.N. Najm, "An Asymmetric SRAM cell to lower gate leakage," in Proceedings of 5th IEEE International Symposium on Quality Electronic Design, 2004, pp. 534-539.

[7]. J.Rabaey, "Digital Integrated Circuits, A Design Perspective", Prentice Hall, Upper Saddle River, NJ, 1996.

[8]. K. Roy and S. C. Prasad, "Low-Power CMOS VLSI Circuit Design", Wiley Publishers, New York, 2000.

[9]. B. Yu *et al.*, "Limits of gate oxide scaling in nano-transistors," in Proceedings of Symposium on VLSI Technology, pp. 90-91, 2000

[10]. "Low Power CMOS Inverter design at different Technologies" International journal of applied engineering research, Dindigul Volume 1, No 3, 201010. "Low Power CMOS Inverter design at different Technologies" International journal of applied engineering research, Dindigul Volume 1, No 3, 2010

[11]. M. C. Johnson, D. Somasekhar, L. Y. Chiou, and K. Roy, "Leakage control with efficient use of transistor stacks in single threshold CMOS," *IEEE Trans. VLSI Syst.*, vol. 10, pp. 1–5, Feb. 2002

[12] C. Gopalakrishnan and S. Katkoori, "Resource allocation and binding approach for low leakage power," in *Proc. IEEE Int. Conf. VLSI Design*, Jan. 2003, pp. 297–302

[13] S. Narendra, S. Borkar, V. De, D. Antoniadis, and A. P. Chandrakasan, "Scaling of stack effect and its application for leakage reduction," *Proc. IEEE ISLPLED*, pp. 195–200, Aug. 2001.

[14] J. Kao, A. Chandrakasan, and D. Antoniadis, "Transistor sizing issues and tool for multi-threshold CMOS technology," in *Proc. 34th DAC*, 1997, pp. 409–414.

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2) Dr.V.Malleswara Rao received his B.E degree from Andhra University in the year 1985 and received M.E degree in the year 1989 from Andhra University and completed his Ph.D from J.N.T.U Hyderabad and working in GITAM Institute of Technology, GITAM University, Visakhapatnam as Professor and H.O.D. He is a life member of AMIE. His research activities are related to Low Power VLSI Design, Microwave, Bio-Signal Processing and EMI/EMC.