Designing and Implementation of Quantum Cellular Automata 2:1 Multiplexer Circuit

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ABSTRACT
Quantum Cellular Automata is a promising nanotechnology that has been recognized as one of the top six emerging technology in future computers. We have developed a new methodology in design QCA 2:1 MUX having better area efficiency and less input to output delay. We have also shown that using this QCA 2:1 MUX as a unit higher MUX can also be designed. We verified the proposed design using simulation from QCADesigner tool. This simulator is also useful for building complex QCA circuits.

General Terms
QCA, Multiplexer

Keywords
Majority voter Circuit, QCADesigner, QCA Cell, QCA 4:1 MUX, Emerging Technology

1. INTRODUCTION
CMOS Technology is approaching its scaling limit very fast. In practical point of view this technology in nano-scales is facing lot of problems. So in order to enhance the performance of a system new nano-technology approach should be taken into account. Quantum Cellular Automata is now one of the promising and emerging technology which not only providing a solution at nano-scale, but also offers solutions that currently CMOS technology is facing[1,2].

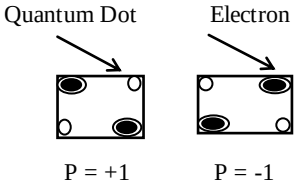
The basic building block of every QCA circuit is majority gate and every QCA circuit can be built using Majority and inverter gate[3]. The majority logic can be implemented in a different manner from that of Boolean logic. The Boolean logic operators(like AND, OR and their complements) and other digital functions can be implemented using Majority logic[4]. The majority logic can be termed as more powerful for implementing digital functions because of very small number of logic gates[5,6].

In this paper we propose a new design methodology for a 2:1 MUX. Using this design as a unit complex MUX design is possible. In comparison to existing implementation, this method has demonstrated significant improvements. The proposed 2:1 MUX resulted in decrease in cell counts and decrease in input to output delay. The presented design is justified using QCA Designer [7] simulation results.

2. DESCRIPTION AND ANALYSIS

2.1 QCA Concept in details
This technology is built up in cells. Each cell has 2 electrons trapped on it and 4 as illustrated in Fig1(a). The electrons can be on any island and can tunnel between the islands. However, due to Coulomb repulsion, they will always settle to one of two stable states. One configuration of charge represents a binary "1, "the other a "0," but no current flows into or out of the cell.

A.



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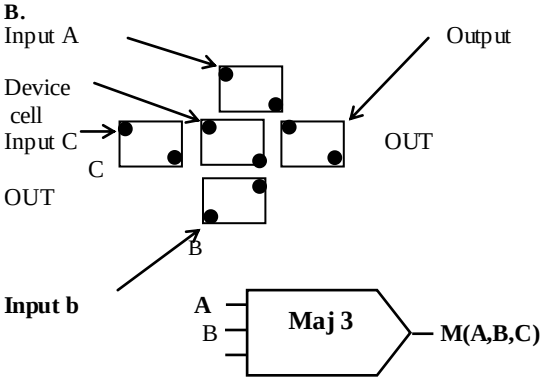

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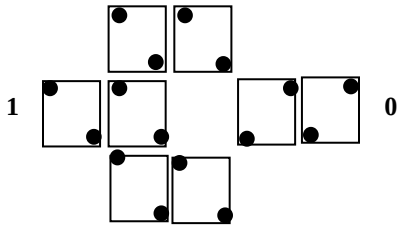


Fig:1 (a) Basic QCA cell and binary encoding, (b) A QCA majority gate and (c) A QCA inverter.

The field from the charge configuration of one cell alters the charge configuration of the next cell. Remarkably, this basic device-device interaction, coupled with a clocking scheme for modulating the effective barrier between states, is sufficient to support general-purpose computing with very low power dissipation. Binary wire can be assembled where all cells in the chain have the same value. The fundamental logic gate is the Majority Gate. A majority gate takes three inputs; its output is equal to whichever two inputs agree as illustrated in Fig 1(b). Assuming three inputs labeled A, B and C, the logic function of majority gate is

$$M(A,B,C)=AB+BC+CA \qquad (1)$$

Logical AND and OR functions can be implemented from majority voter by presetting one input immutably to binary values 0 and 1, respectively. A signal is complimented by the not gate as in fig 1(c).

2.2 Advantages of QCA

- This technology has many advantages. It is "edge driven," meaning an input is brought to an edge of a QCA block; it is evaluated and output at another edge. This also means that no power lines need be routed internally.
- The second advantage is that QCA systems should be very low power, because there is no current flowing. Only enough energy needs to add to lift the electrons from their ground states.
- Finally, QCA cells are very small.

2.3 QCA Clocking

The clocking of QCA [10] can be accomplished by controlling the potential barriers between adjacent quantum-dots. When the potential is low the electron wave functions become delocalized resulting in no definite cell polarization. Raising the potential barrier decreases the tunneling rate, and thus, the electrons begin to localize. As the electrons localize, the cell gains a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched. Latched cells act as virtual inputs and as a result, the actual inputs can start to feed in new values. This enables easy pipelining of QCA circuits. It has been shown that four clocking zones each Pi / 2 degrees out of phase is all that is required by any QCA circuit as shown in Figure 2.

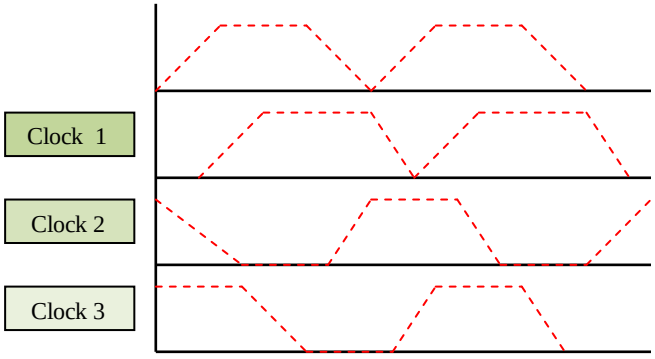


Fig: 2 QCA Clocking

3. EARLIER WORK

The Paper [11] proposed a whole new design of a QCA 2:1 MUX. A modular design which can be used to extend 2:1 multiplexer QCA layout to larger 2^n multiplexer layouts, using the elementary building blocks has been proposed.

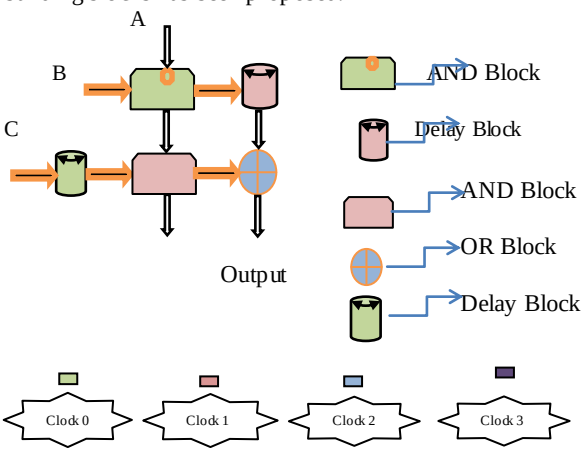
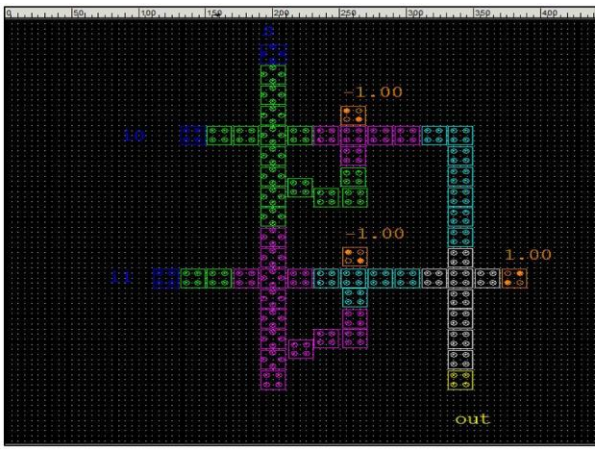


Fig 3: Block diagram of 2:1 MUX

Their objective is to develop a modular design methodology which can be used to design 2^n to 1 multiplexers using building blocks. To meet this specification the design must consist of elementary blocks properly selected so that can be used to build larger 2^n:1 multiplexers. A high-level block diagram of the 2:1 multiplexer design is shown in Fig 3, where B and C are the multiplexer signal inputs, A corresponds to the selector input and out is the multiplexer output signal. The design includes an AND block, an (a. b') AND block and an OR block. It also includes one signal delay block at the C input of the circuit. All blocks are colored according to the clock they use. It can easily be seen that the clocking phases are traversed in the proper order (0, 1, 2, 3, 0, 1 …) so that the required clock phases are always adjacent to one another to allow for correct signal propagation. The signal propagates diagonally with a line profile from the top left block to the bottom right block which is the output block. Using this pipelining structure the proper signals arrive simultaneously at the inputs of the AND and OR blocks. The signal delay block must exist at the C input in order to synchronize the first column AND block west input signal, with the A signal coming from the north input which already has been delayed from the previous level AND block.



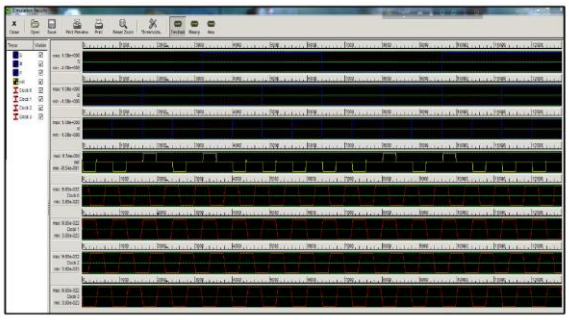
Circuit Specifications:

- No of cells=63
- Cell size=18*18 nm.

- Cell area= 63*18*18 sq. nm.=20412 sq. nm.
- Spatial Dimension=238 nm. long & 280 nm .wide
- Area Covered=66640 sq. nm.
- % Area Usage=30

Fig 4: Circuit diagram and Circuit specification for earlier 2:1 MUX unit

Simulation Results:



(This is the simulation results we encountered while executing the previous circuit)

Fig 5: Simulation Result of the previous circuit.

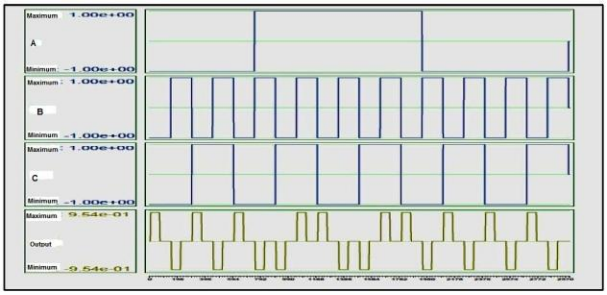
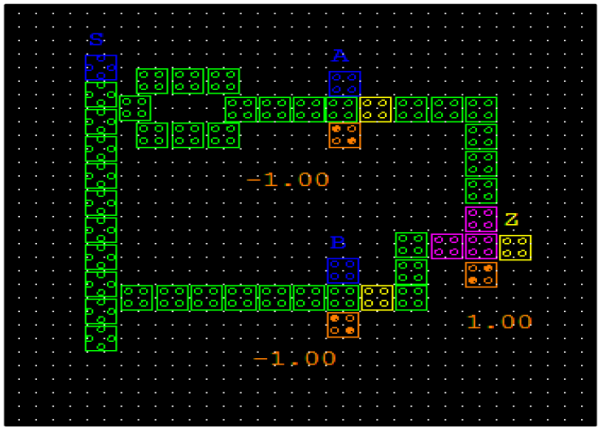


Fig 6: Simulation Results given in the paper [11]

4. PROPOSED WORK

As we have found a clear disagreement in between two simulation results, in immediate manner we started looking for a new design methodology for 2:1 MUX which is very simple but very efficient. For the same we have tried a conventional approach, we used two AND gates for AND ing two inputs with the selection line and One OR gate to add them.



Circuit specifications:

- No of cells=49
- Cell size=18*18 nm.
- Cell area= 49*18*18 sq. nm =15876 sq. nm.
- Spatial Dimension=238 nm. long & 280 nm. wide
- Area Covered=66640 sq. nm.
- % Area Usage=34

Fig 7: Circuit diagram and Circuit specification for proposed 2:1 MUX unit

Simulation Results:

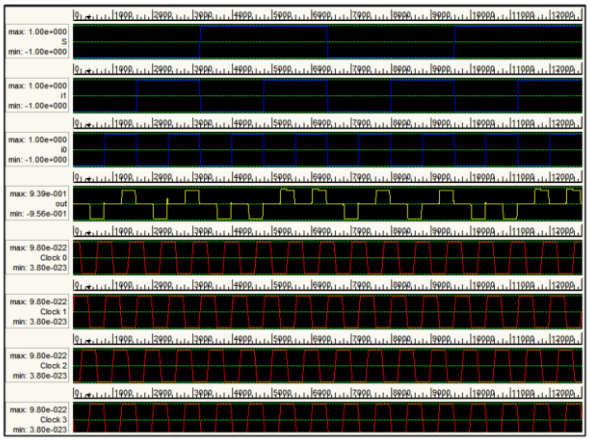


Fig 8: Simulation Result of the previous circuit.

Table 1: Comparative study of two Designs

Parameters	Earlier 2:1MUX	Proposed 2:1	Percentage Reduction
No of Cells	63	49	22.2
Total area	66640 Sq nm	46332 sq nm	30.47
Cell area	20412 Sq nm	15876 Sq nm	22.2%
Area Usage	30%	34%	4% extra
Input to output delay	Four clocking Zone	Two clocking Zone	50

As we had impressive result with our proposed circuit, we were ready to develop a higher mux using our proposed 2:1 MUX as a modular set. In the Fig 9 we designed 4:1 MUX using our proposed 2:1 MUX as a modular unit.

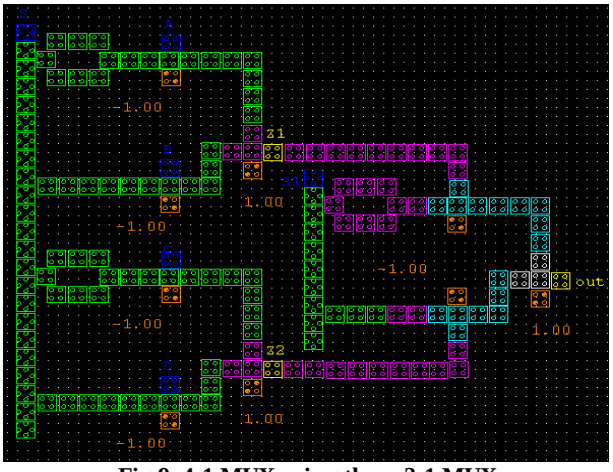


Fig 9. 4:1 MUX using three 2:1 MUX

In this circuit we have used three 2:1 MUX among them two are directed by a single common selection line, and output of those two are fetched into the inputs of third 2:1 mux having a different selection line.

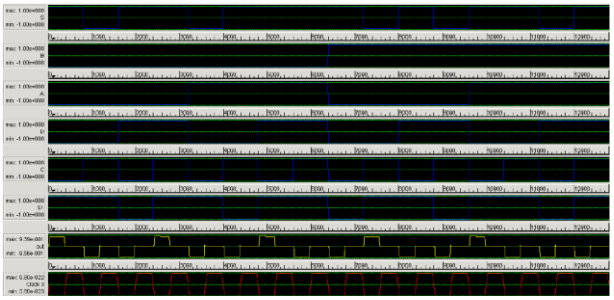


Fig 10: Simulation result of 4: 1 MUX

5. CONCLUSION

Our proposed methodology is an efficient way that greatly reduces no of cells, area and delay in signal propagation from input to output. By this methodology we can go for designing complex multiplexers. This methodology is very simple to implement also. This QCA technology is the future nanotechnology and different classical models can be replaced by this QCA logic and this will become much more efficient and less complex than its classical counterpart.

6. REFERENCE

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