Design of Homogeneous Multi-Core based Vehicular Embedded Controller

Rahul K. Hiware
Research Scholar

Abhijit S. Titarmare
Research Scholar

Dr. Dinesh Padole
Professor

Dr. Preeti Bajaj
Professor

Department of Electronics Engineering,
G. H. Raisoni College of Engineering, Digdoh Hills, Nagpur, India 440016

ABSTRACT

Increasing use of Electronic gadget in vehicular system need researchers' attention to provide optimize solution for the system; in various aspects like power consumption, size, cost, complexity etc. There are many economic and technical arguments for the reduction of the number of Electronic Control Units (ECUs). One can be number of nearby applications of homogeneous or heterogeneous nature can be controlled by one ECU. The use of multi-core technology gives facility to put multiple cores depends on the applications in to single die with their peripherals.

The paper presents design of multi-core embedded controller for vehicular system. Two Leon processor cores connected with AMBA shared bus with memory and peripherals. Some vehicular applications are modeled on the designed system. The modeling of dual core embedded system and application are presented in the paper with their simulation results

General Terms

Multi-Core Embedded System, Vehicular Controller.

Keywords

Multi-Core, Vehicular System, LEON3, Leon Processor, Intelligent Transport System.

1. INTRODUCTION

Vehicular electronics systems have changed radically over the last two-three decades. Early vehicular electronics systems were made up of switches, wires, relays and controlled motors or lamps. Modern vehicles however incorporate a wide range of sensors and actuators coupled to advanced electronics control system. The main motivation behind this is because of fast response, lower cost, reduced weight, new and innovative functionalities, most user-friendly and faster design cycles. The work presented here, deals with the design of a Vehicular application for an electronic control using LEON3 processor.

Fast growing automatic design technology, manufacturing process of semiconductor and market demand for miniaturization of electronics systems, leads different functional systems put into one chip called System-on- Chip (SoC) [1][2]. SoC or a multi-core system offers an immediate and cost-effective technology for solving today's processor design challenges, alleviating the byproducts of heat and power consumption that exist when continually advancing single core processor frequency, or 'clock speed'. Multi-core processors have the potential to run applications more efficiently than single-core processors, giving users the ability to keep working even while running the most processor intensive tasks in the background.

The division of Vehicular Systems has a clear focus on control, diagnosis, and supervision of functions in vehicles. The overall aim is to develop control systems to obtain performance, safety, energy utilization, and environmental stability. To achieve this, there is a requirement to continuously monitor and control various important parameters of a vehicle. These parameters are mainly engine performance, fuel level, battery level, electronic power train, speed, car information system, accidental protection system etc. All of these parameters are controlled and monitored continuously by using electronic system with supporting mechanical assembly in the Car. This electronic system is known as Electronic Control Unit (ECU).

This paper presents Embedded Controller design using; resource sharing based multiple LEON processors for controlling some vehicular applications. Those applications are discussed here. To meet the growing needs of computing power, communication speed and performance requirements demanded by today's applications, processor clock speed has to be increased. However, increasing clock speed is not viable anymore due to heat dissipation and power consumption constraints. Hence Instead of trying to increase the clock speed, multi-core processor architectures with the lower frequency can be used.

A multi-core processor is a single integrated circuit in which two or more processors have been attached for enhanced performance, reduced power consumption and more efficient simultaneous processing of multiple tasks. A processing system is composed of two or more independent cores. An individual Processor is called as Core. The cores are integrated onto a single integrated circuit die or multiple dies in a single chip package. Multi-core system does implement multiprocessing in a single physical package.

LEON is a 32-bit CPU microprocessor core, based on the SPARC-V8 RISC architecture and instruction set. It was originally designed by the European Space Research and Technology Centre, part of the European Space Agency, and after that by Gaisler Research. It is described in synthesizable VHDL. LEON has a dual license model: A LGPL/GPL FLOSS license that can be used without licensing fee, or a proprietary license that can be purchased for integration in a proprietary product. The core is configurable through VHDL generics, and is used in system-on-a-chip (SoC) designs both in research and commercial settings. The LEON3 is a synthesisable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The model is highly configurable and particularly suitable for SoC designs [3].Proposed architecture is based on AMBA (Advance

Microcontroller Bus Architecture) AHB/APB shared buses, to which new module of processor or peripherals can easily be added. It is a single resource which can carry only one transaction at a time. Hence to resolve the issue of bus sharing among multiple masters arbitration policies are to be used. Round robin and fixed arbitration policies are included in the design. Peripherals are also shared among various maters [4].

2. EMBEDDED CONTROLLER DESIGN

The Embedded controller discussed in this paper is designed to monitor and control the various applications in vehicular system. Vehicular system as discussed earlier has various parts like mechanical controlling parts operated mechanically or electronically. Monitoring of various parameters like fuel level, battery charging, speed measurement, temperature.

The aim is to design an application for vehicular system using multi-core embedded controller. The application uses many sensors and the actuators. Sensors are input to the controller and actuators are output of the controller. It is mainly consists of monitoring the parameters by sensors and according to controller program actuators will control the respective parameter.

2.1 Design

Fig.1 shows the block diagram of an application for vehicular system. The sensors here used are

- Temperature sensors : Placed inside vehicle, to monitor temperature inside vehicle
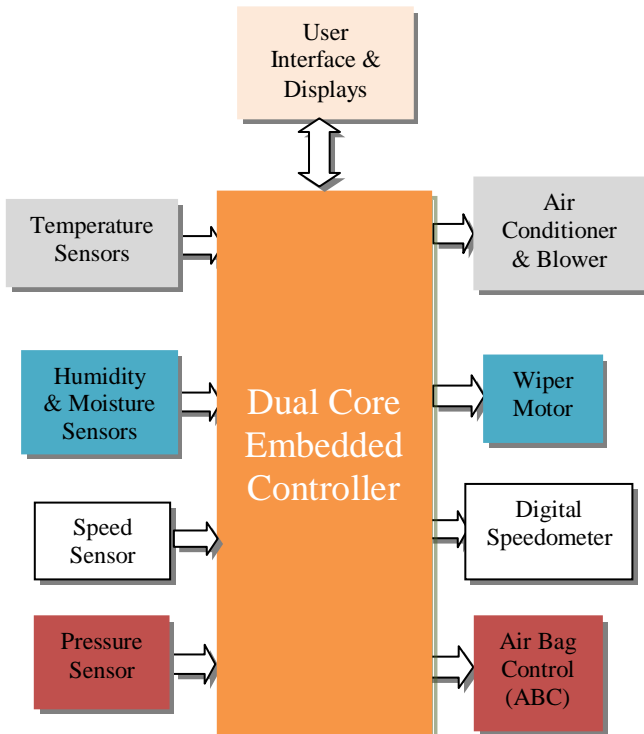
Fig.1 Block diagram of an application for Vehicular System

Actuators or controlling parts are mainly switches to ON/OFF mechanical assemblies or to drive the motors.

- Humidity & Moisture sensors : Placed on boundary of windshield, to check water droplets on windshield
- Pressure sensors : Place on front buffer and bonnet, to detect dash or collision
- Speed detector: on the rear wheel axel
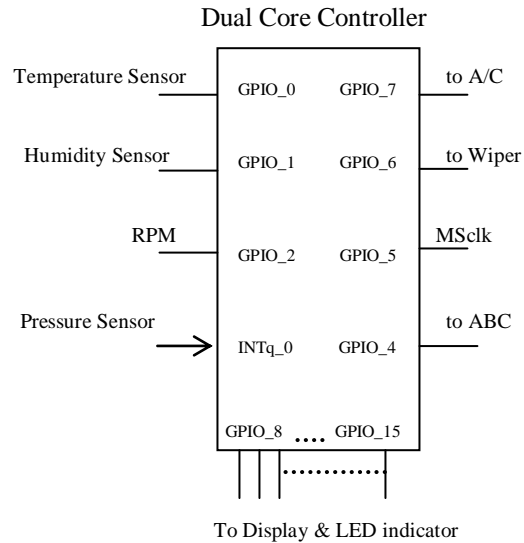
Fig.2 Connection Diagram for vehicular system

- A/C : to maintain inside temperature
- Wiper motor : to move wipers
- Air bag control: for driver's protection
- Digital speedometer & Display : on the dashboard

There will be various displays showing speed in digital form, fuel level indicator, battery charging level, engine temperature, A/C indicator, hand break indicator, headlight upper/dipper, etc.

2.2 Working

Temperature is sensed by a temperature sensor, compared with upper and lower limits by controller and according to logic cool or hot air will be blowed on engine to maintain temperature. Humidity sensor will sense the presence of droplets or rain drops and activate wiper motor. Odometer is used for speed measurement. Pressure sensors are used for any dash or accident occurs air bag will pop out for protection of driver.

Fig.2 shows the connection diagram for the projected application. GPIO stands for general purpose input/output ports, INTq_0 is interrupt pin and MSclk is master to slave clock for communication between sensors and controller. Methodology used to design controlling application is mainly divided in Hardware and Software categories which are explained next.

3. HARDWARE DESIGN

Hardware part defines the design of a dual core controller. Embedded controller consists of processor with memory and Peripherals. The dual core controller is designed using two LEON3 processor cores. Peripheral on chip can be Timer, serial communication interface, Interrupt controller and programmable IO devices. The system design presented here have used shared bus (AMBA Bus is utilized for core interface) and shared resources (peripherals and Memory).

The embedded controller designed here is Homogeneous Tightly Coupled multi-core architecture. Fig.4 [5] shows block diagram for embedded controller. In the diagram LEON-0 (CPU_0) and LEON-1 (CPU_1) are LEON3 processor core. Each processor has their individual cache memory. Both cores (CPU_0, CPU_1) are connected using AMBA shared bus. Leon '0' is configured as boot processor.

3.1 Synthesis Results

Fig.5 shows the resources used by multi-core vehicular embedded controller on Virtex5 target device (XC5vlx30-3ft324). It is the synthesis report of Multi-Core (Dual-Core in this case) Vehicular Embedded Controller, generated in Xilinx ISE 9.1i.

Fig.6 shows the RTL structure of dual-core LEON3 system RTL view is obtained after configuration of IP core and synthesis in Xilinx ISE 9.1i for the block diagram explained in fig.4.

3.2 Simulation Results

Fig.7 is showing simulation waveform of the AMBA bus operating in an embedded controller. It also shows the configuration of AMBA-AHB & APB for master and slaves.

Fig.8 (a) shows the value disassembly of embedded controller on ModelSim consol. It is showing a data transfer instructions executing to transfer value 0x00003FFE on the output port of a controller. Fig.8 (b) shows its waveform; transfer of value takes place at 303370ns and it can be seen in waveforms at the same time.
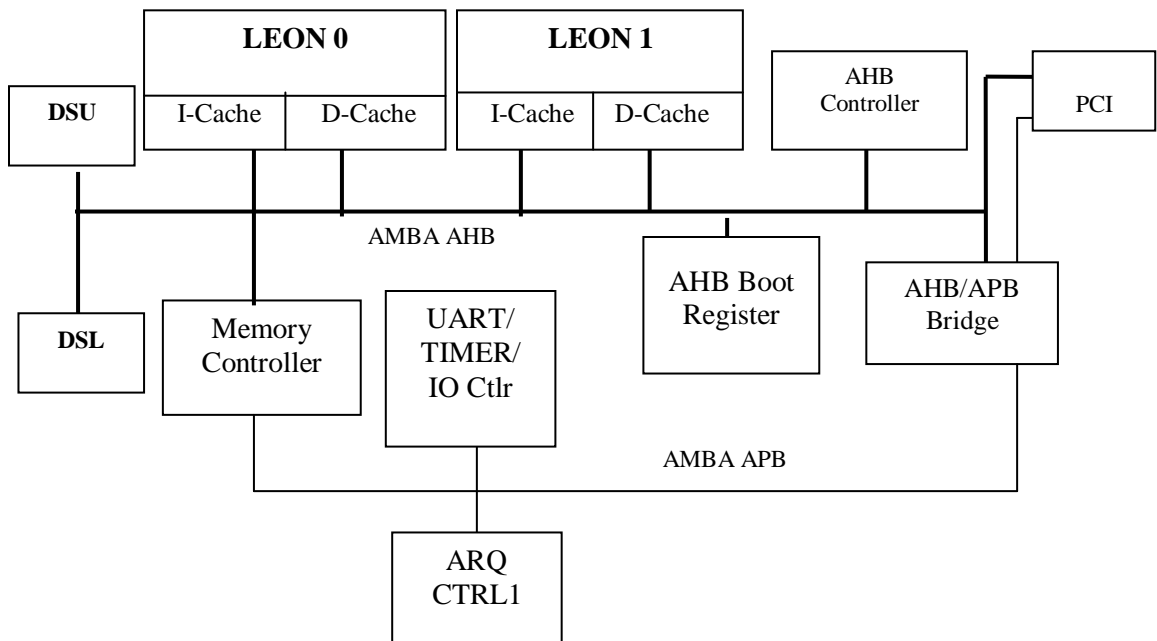
Fig.4 Block diagram of Dual core LEON3 System

TRY29DEC'10 Project Status			
Project File:	try29dec'10.ise	Current State:	Synthesized
Module Name:	leon3mp	• Errors:	No Errors
Target Device:	xc5vlx30-3ff324	• Warnings:	11888 Warnings
Product Version:	ISE 9.1i	• Updated:	Wed Jan 26 18:23:46 2011

Current Errors
No Errors Found

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	6213	19200	32%
Number of Slice LUTs	11687	19200	60%
Number of fully used Bit Slices	3631	14269	25%
Number of bonded IOBs	113	220	51%
Number of Block RAM/FIFO	8	32	25%
Number of BUFG/BUFGCTRLs	1	32	3%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed Jan 26 18:23:18 2011	0	11888 Warnings	118 Infos

Fig.5 Snapshot of Synthesis Report generated for Multi-Core Vehicular Embedded Controller
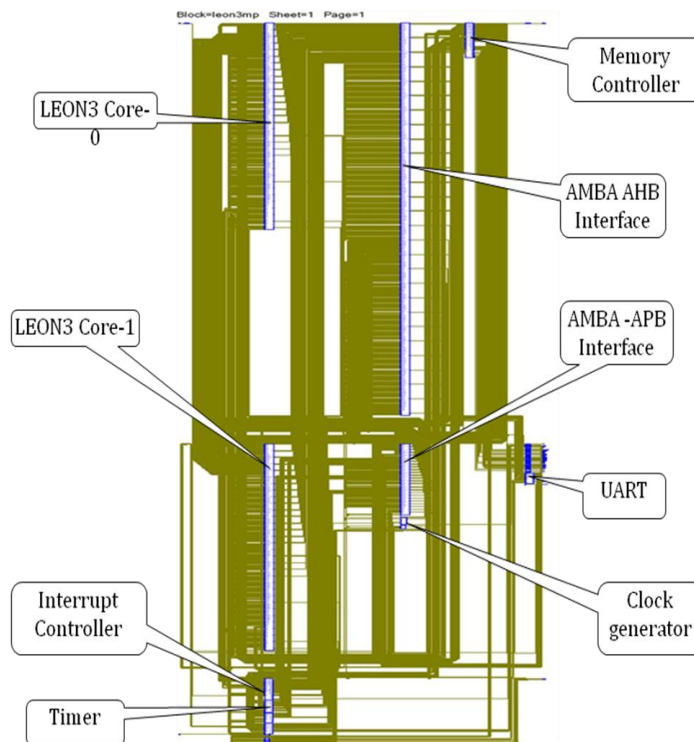
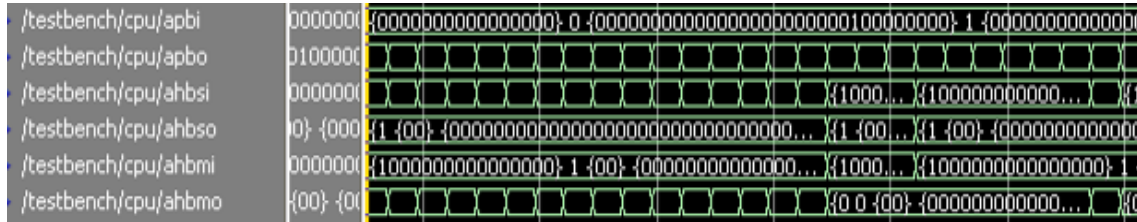**Fig.6 RTL Structure of multi-core Vehicular Embedded Controller**

Fig. 7 Simulation Waveforms showing AMBA shared buses - AHB & APB
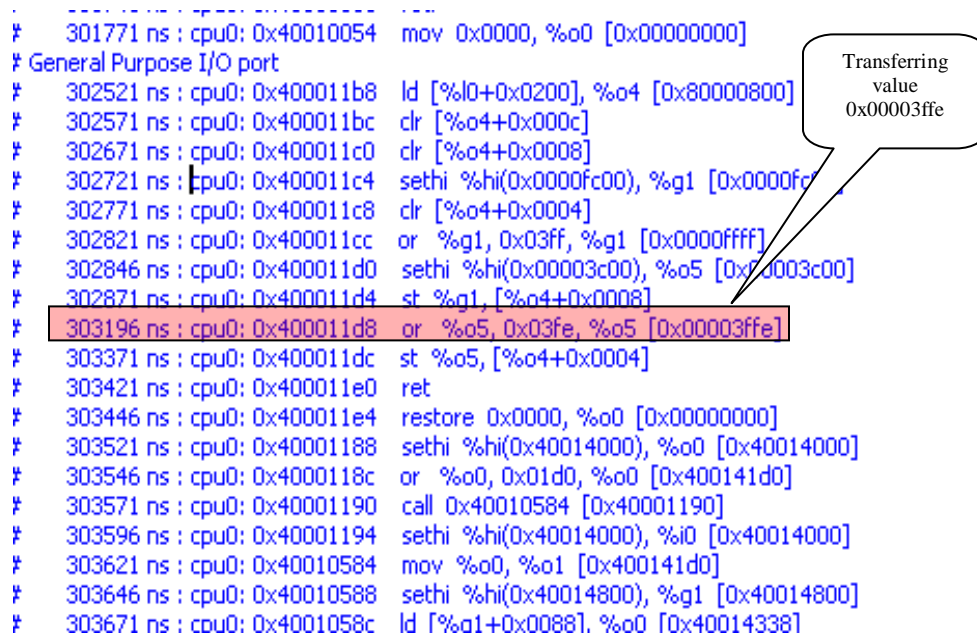

Fig. 8 (a) Date Transfer SPARC V8 Instructions executing in Dual-Core Embedded Controller
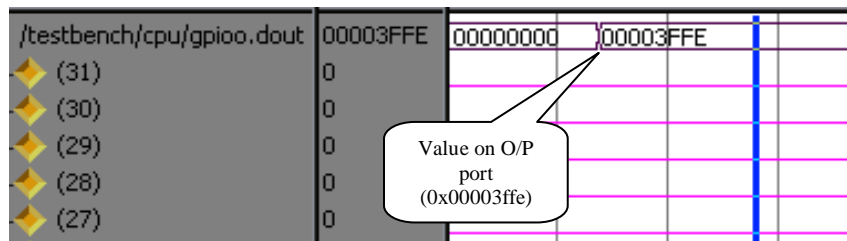

Fig. 8 (b) Output Value 0x00003FFE on ports of Embedded Controller

4. SOFTWARE DESIGN

The advanced electronics control system required to be fast design to market time to rip the advantage of time. This leads the designer to use some advanced tools like simulator and debugger. Applications explained above for this architecture are simulated on TSIM simulator for LEON processor.

TSIM is a generic SPARC architecture simulator capable of emulating ERC32- and LEON-based computer systems. TSIM supports solaris-2.8, Linux, linux-x64, Windows 2K/XP, and Windows 2K/XP with Cygwin UNIX emulation. The LEON port of Snap Gear supports MMU and non-MMU LEON configurations, as well as the optional V8 mul/div instructions and floating-point unit (FPU). The ports include symmetric multi-processing (SMP) support for LEON3 systems with multiple processors. TSIM environment of LEON processor executes .exe files generated in sparc-elf software. Sparc is v8 instruction set which supports the TSIM simulator. BCC is a cross-compiler for LEON2 and LEON3 processors. It is based on the GNU compiler

tools and the Newlib standalone C-library. The cross-compiler system allows compilation of sequential (non-tasking) C and C++ applications.

4.1 Air Conditioner control

Air conditioner control allows controlling the ambient temperature in vehicle based on the drivers and passengers requirements. The air conditioner controller is programmed to contact air conditioning and heating systems in vehicle directly. Fig 9 shows flow chart for the air conditioner control to maintain the temperature inside vehicle.

Fig 10 shows snapshot for air conditioner control, program is simulated in TSIM.
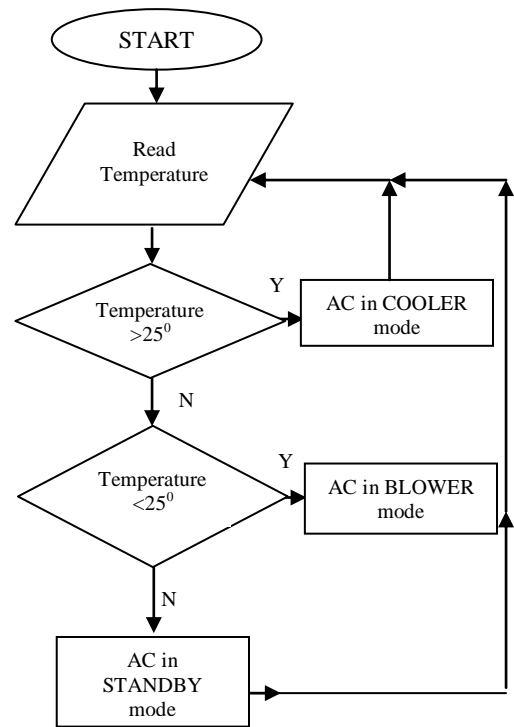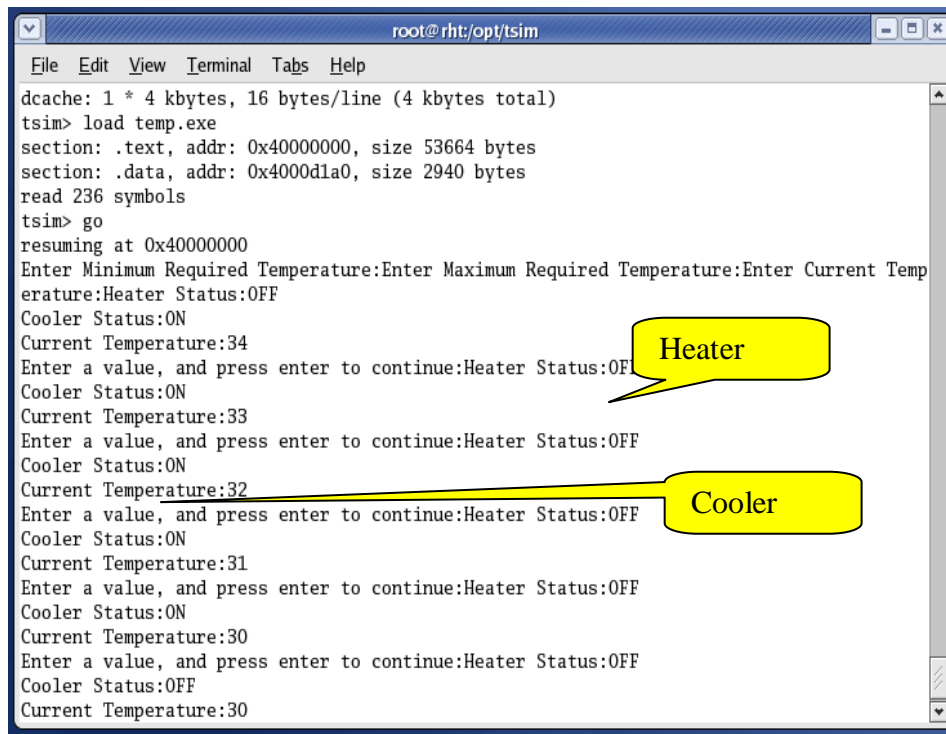
Fig.9 Flow chart of Air Conditioner Control

Fig.10 Simulation result for Air Conditioner Control application.

4.2 Wiper control

A windscreen wiper or windshield wiper is a device used to remove rain and debris from a windscreen or windshield. Almost all motor vehicles are equipped with such wipers, which are usually a legal requirement.
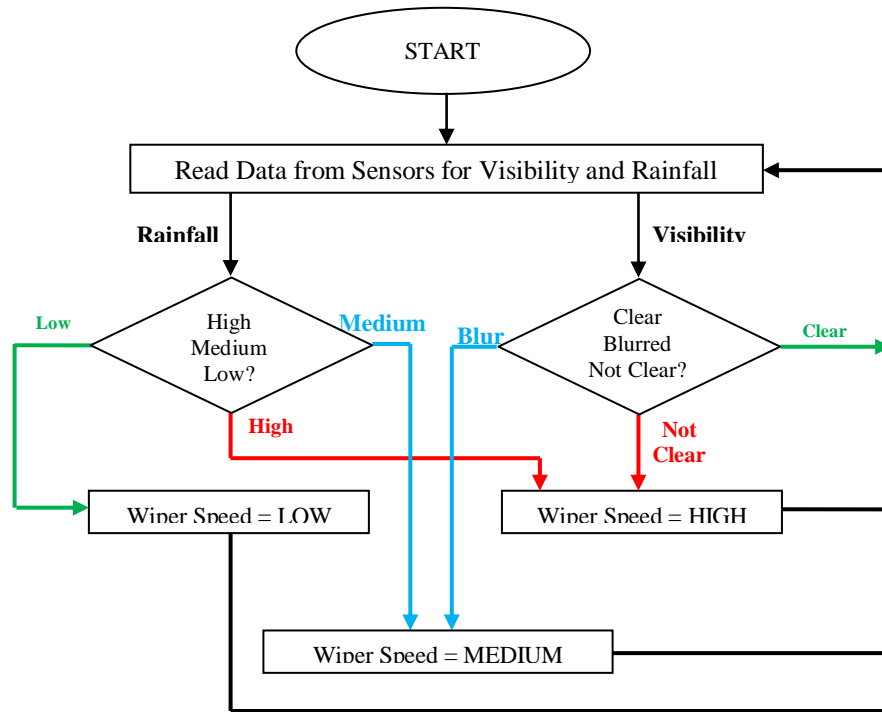

Fig.11 Flow chart of Wiper Control application

Fig.12 Simulation Result for Wiper Control application

5. CONCLUSION

The homogeneous multi-core Vehicular Embedded Controller has design and tested. The objective of building a customizable Muli-Core (Dual-Core in this case) System SoC is successfully accomplished.LEON3 processor core is used with shared resources like AMBA bus and shared memory for designing the said system. Some of the applications of vehicular system are also simulated in TSIM for the same.

Proposed design can be used for developing user defined embedded controller for performing dedicated task. Applications particularly in the domain of Image Processing, Computer Vision, wireless networking and multimedia inherently possess great amount of functional and data parallelism, which can be exploited through a proposed Multi-Core System.

The present symmetric, general purpose Homogeneous Multi-Core System can be replaced by Heterogeneous Multi-Core System by means of which degree of functionality can be increased (Different functional unit can perform different operation).Hybrid ASIC may be the future of cheap SoC. Standard Cell technology allows the development of System-on-Chip (SoC) units to feature enhanced performance and small sizes, though requiring a lot of time and money, which would make the business less profitable.

Introduction of Real Time Operating Systems (RTOS) in the proposed work can be very useful not only in Intelligent Transportation System (ITS) but also in various high end applications like Aircraft Simulations, 3-D games, Video Processing, High end electronic gadgets and Defense applications.

6. REFERENCES

[1] S. Guccione, "Simulating a Mulitcore Supercomputer", in Austin Conference on Inte-grated Circuits and Systems (ACISC), May 2007.

[2] A. Patel, C. Madill, M. Saldana, C. Comis, R. Pomes, and P. Chow, "A Scalable FPGA- based Multiprocessor", in 14th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, April 2006, pp.111,120.

[3] Jiri Gaisler. *The LEON-3 Processor User's Manual,* Version 1.0.20, February 2009 http://www.gaisler.com,

[4] ARM Limited, AMBA specification, 2.0 editions, 1999, © ARM Limited.

[5] *Snehal Dongare, Dinesh Padole, Dr. Preeti Bajaj,* "Design of Shared Resource Based Multicore Embedded Controller Using LEON Processor", ICETET-10, Goa, India.

[6] *Dinesh Padole, Dr. Preeti Bajaj, "*Fuzzy Arbiter Based Multi Core System-On-Chip Integrated Controller for Automotive Systems: A Design Approach", IEEE CCECE08, Canada.

[7] Renesas Electronics Corporation,© 1995-2011 All rights reserved http://www2.renesas.com/applications/en/automotive/enviro nment/eco/index.html, accessed April 2011

[8] Jason G. Tong, Ian D. L. Anderson and Mohammed A. S. Khalid, "Soft-Core Processors for Embedded Systems", 18th International Conference on Microelectronics (ICM), Dhahran, Saudi Arabia, December 2006.

[9] IBM, QuadCore, http://www-03.ibm.com/systems/x/quadcore.html, accessed on December 2010

[10] Dual-Core Intel® Xeon® Processor, "Increasing Data Center Density While Driving Down Power and Cooling Costs" www.intel.com/go/xeon

[11] http://www.1-core.com/library/digital/soft-cpu-cores/, accessed on December 2010

[12] Prof. Anshul Kumar and Prof. M. Balakrishnan. *A Methodology for Synthesis of ASIP based Multiprocessor SoCs*. Department of Computer Science and Engineering, IIT Delhi, 2002.

[13] John Fruehe " Planning Considerations for Multi core Processor Technology", www.dell.com/powersolutions

[14] SPARC International Inc, SPARC International Inc, 535 Middlefield Road, Suite 210, Menlo Park, CA 94025. *The SPARC Architecture Manual Version 8*, 1992.

[15] John Hennessy & David Patterson. *Computer Architecture: A Quantitative* 56 *Approach, 2nd edition*. Morgan Kaufmann Publishers Inc, San Francisco, California, 1996.

[16] Vijay S. Pai, Parthasarathy Ranganathan, and Sarita V. Adve. *RSIM Reference Manual Version 1.0*. Technical Report 9705, Department of Electrical and Computer Engineering, RICE University, August 1997.