Compact CPLD Board Designing and Implemented for Digital Clock

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ABSTRACT
The work describes the design and implementation of Complex Programmable Logic Devices (CPLDs) board for many digital applications in the educational and research field laboratory in the university. The objective of designed board is to implement the digital logic, which can be used for any digital application and take advantages of CPLDs features like reconfigurable architecture, high speed operation, pin locking, in-system programming (ISP) for digital system design. This CPLD board size is relatively compact; so it can be easily mounted. On board power supply and variable frequency oscillator improves functionality of overall board. The design includes some cost effective embedded control and communication interface to build digital application to work more efficiently in the market.

Keywords
Reconfigurable architecture, CPLD, Digital Design, Digital Clock, PLDs.

1. NTRODUCTION
The process of designing digital hardware has changed dramatically over the past few years. Unlike previous generations of technology, in which board-level prototype designs included large numbers of SSI chips containing basic gates, virtually every prototype digital design produced today consists mostly of programmable logic devices [7]. This applies not only to digital logic circuits, but also for robotics applications like sensing, actuation, manipulation. Programmable logic offers the digital circuit designer the possibility of changing design function even after it has been built. A programmable logic device (PLD) can be programmed, erased, and reprogrammed many times, allowing easier prototyping and design modification. PLDs can be programmed from personal computer (PC) or workstation running special software. This software is often associated with a set of programs that allow us to design circuits for various PLDs [2].

For successful implementation of digital design and, it is essential to have suitable CPLD board for teaching and learning CPLD programming as well as for real time application development. It should be affordable, user friendly and flexible. The following sections describe the design of the CPLD board, application of the board, the benefits of the board, and finally concluding remarks. The implementation of the CPLD board used here is digital clock. The complete module consists of many sub modules of onboard and in CPLD chip like power supply, variable frequency crystal oscillator and I/Os are onboard and counter, multiplex, decoder, and comparator are designed inside the CPLD chip. The time displayed is in the form of binary coded decimal and seven segments.

2. BOARD SPECIFICATION
CPLD architecture is suitable for designing medium capacity digital systems. Our work is focused on XC9572 CPLD chip from Xilinx, which can obtain 72 macro cells with 1600 logic gates; which is sufficient for performing various laboratory experiments. CPLD board block diagram and designed CPLD board is shown in Fig. 1 and Fig. 2 respectively.

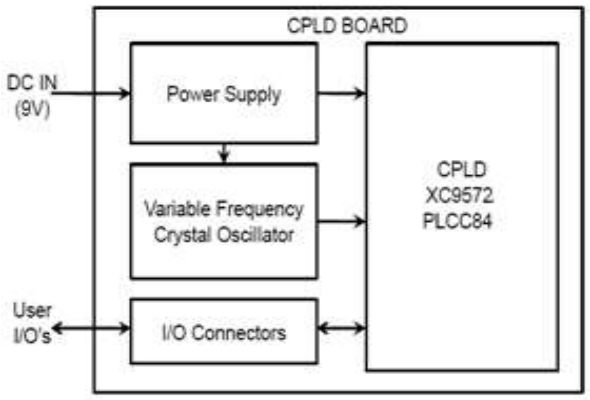

Figure 1. Block Diagram of CPLD

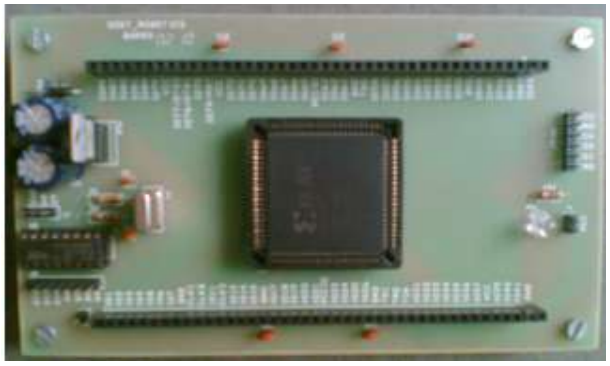

Figure 2. Designed CPLD Board

CPLD board consists of four units as follows:

- CPLD
- Variable frequency crystal oscillator
- Power supply
- Inputs / Outputs connectors

Brief idea of these individual units is provided in following sub-topics.

2.1 Complex Programmable Logic Devices

Xilinx manufactured XC9572 CPLD provides advanced in-system programming and test capabilities for high performance, general purpose logic integration. All devices are in-system programmable for a minimum of 10,000 program/erase cycles. Extensive IEEE 1149.1 (JTAG) boundary-scan support is also included on all family members. The XC9572 architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. I/Os may be configured for 3.3V or 5V operations. All outputs provide 24 mA drives [4].

The XC9572 CPLD has four different pin packages: 44-pin PLCC, 84-pin PLCC, 100-pin PQFP, and 100-pin TQFP. Microcells are functional blocks that perform combinatorial or sequential logic. XC9572 device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the Fast CONNECT switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with 36 inputs and 18 outputs. The Fast CONNECT switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, 12 to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs [3]. XC9572 architecture is shown in Fig. 3.

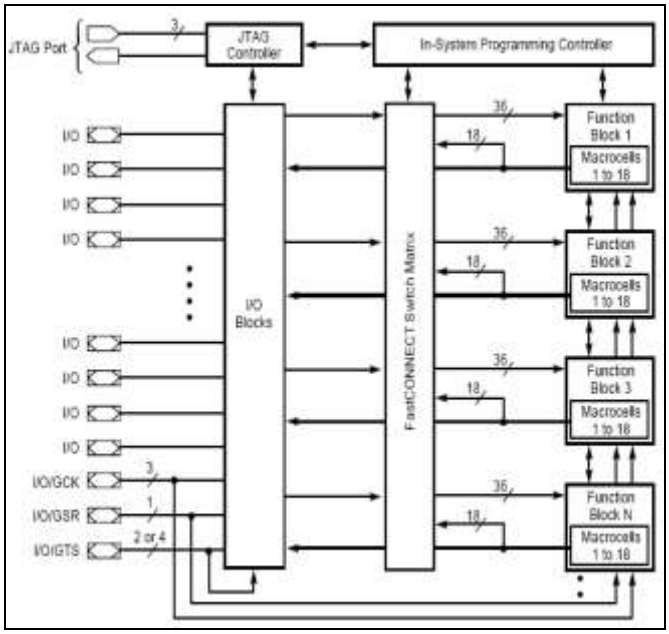

Figure 3. Architecture of CPLD 9572

2.2 Variable Frequency Crystal Oscillator

CPLD XC9572 with PLCC 84 package having three clock inputs (clk1, clk2, and clk3). We can provide two different clock inputs i.e. clk1 and clk2 from in- build variable frequency oscillator. This variable frequency oscillator can provide maximum clock frequency up to 25MHz at room temperature.

We are using crystal and IC 74HC4060 for designing variable frequency oscillator as shown in Fig. 4. The 74HC4060 consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits [6].

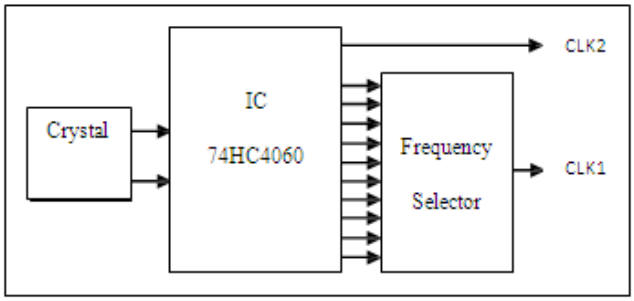

Figure 4. Variable frequency crystal oscillator

2.3 Power Supply Unit

Commercial grade CPLDs XC9572 with PLCC 84 pin requires supply voltage between 4.75V to 5.25V [3]. We have designed power supply unit using LM7805 regulator IC; which provides 5V regulated output with output current of 1A. Power supply indicator LED is connected at the output of LM7805. Power supply unit requires DC 7.5V to 15V input. Block diagram of power supply unit is shown in Fig. 5.

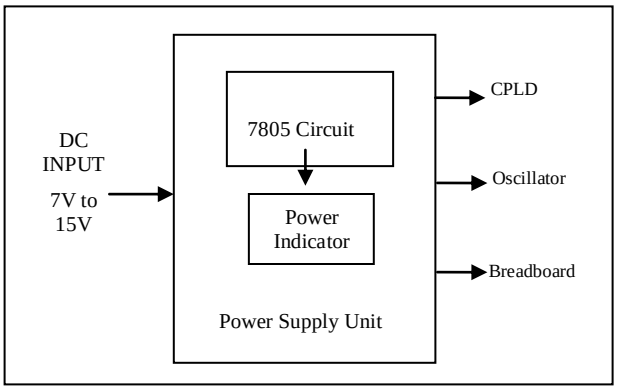

Figure 5. Power Supply Unit

3. SOFTWARE SUPPORT

XC9572 CPLD board is fully supported by the development systems available from Xilinx and the Xilinx Alliance Program vendors. The designer can create the design using ABEL, schematics, equations, VHDL, or Verilog in a variety of software front-end tools. The development system can be used to implement the design and generate a JEDEC bitmap which can be used to program the XC9572 device. Each development system includes JTAG download software that can be used to program the devices via the standard JTAG interface and a download cable [3]. We are using Xilinx ISE Webpack platform for developing system on CPLD XC9572. Xilinx ISE Webpack is freely available tool; which can be easily downloaded from Xilinx website. We are using parallel port JTAG download cable; to program CPLD from personal computer. This cable is developed with minimal components compared to Xilinx Parallel Cable III. Only disadvantage of this cable is that we cannot extend its length more

than 30cm. Implemented JTAG download cable is shown in Fig. 6.

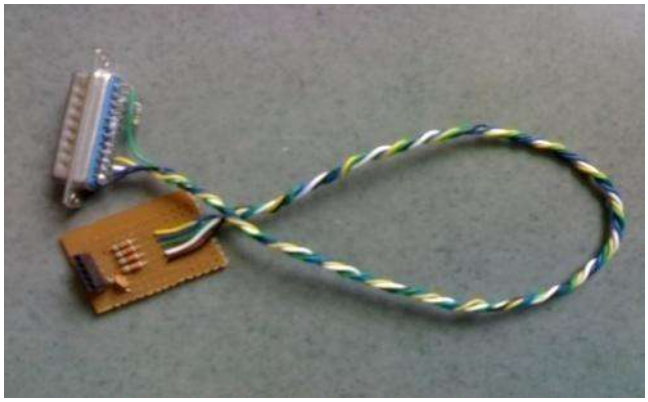

Figure 6. JTAG download cable

4. DESIGN OF DIGITAL CLOCK

4.1 Software

The design of the digital clock is done in VHDL. The sub modules in the main module of the identity of the clock are counter, multiplexer, decoder. The entity and block diagram of the clock is shown in Fig. 8 and Fig. 9 respectively. The inputs for the module is clock, reset and the outputs of the module are seven segments display, binary coded decimal like hours, minutes and seconds. The clock frequency of onboard is divided into one second pulse by clock divider block, and then this clock is fed to the counter which counts hours, minutes and seconds. The counter output is fed to multiplexer and binary coded display led's. Then this output is fed to the multiplexed seven segments. The multiplexer and multiplexed seven segments are connected together with the help of decoder. The time is displayed correctly on the seven segment led's. The input id pins are used to adjust the time when it is initially started i.e. when it is switched on.

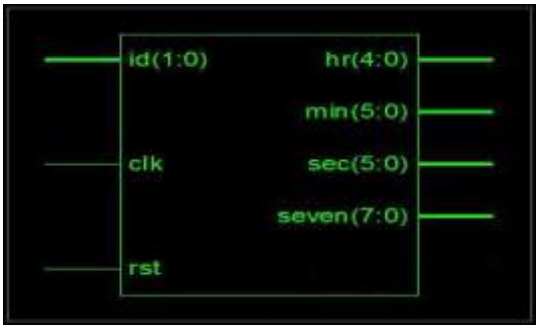

Figure 7. Entity of the Digital clock

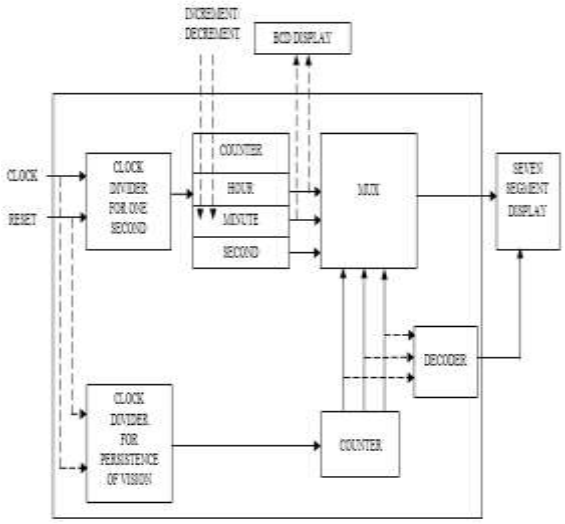

Figure 8. Flow chart for digital clock design

4.2 Hardware

The design of digital clock consists of CPLD board, seven segment leds to display hour, minute and second, eight bit led display for binary coded display. The clock used from the external variable crystal is one second at the pin 14 of 74HC4060 fed to the CPLD. The front view of digital clock is shown in Fig. 7.

The eight bit led display is arranged with a common anode, so the CPLD is working in a sinking mode to glow leds. The seven segment leds are multiplexed with common address lines and arranged in common anode mode, so that CPLD can work on sinking mode.

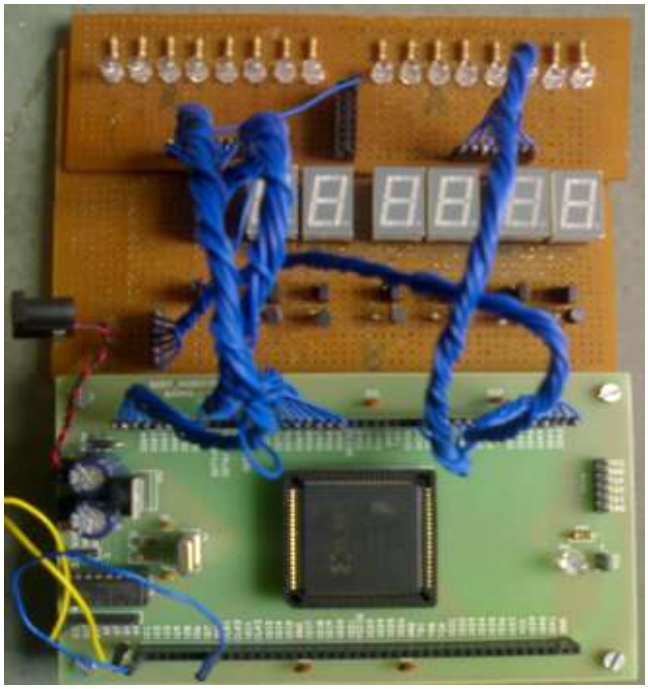

Figure 9. Front View of Digital clock Design

4.3 Synthesis Report

Here, we are using Xilinx XC9572 device from XC9500 CPLD family with PLCC 84 package. It includes 72 macro cells with 72 I/O's. The CPLD contains complete digital logic with both facility of binary coded display and seven segment display. The synthesis report table of digital clock is shown in Table1.

Table1. Resource used on CPLD by Digital clock

Macro cells used	Pterms used	Registers used	Pins used	Function block i/ps used
60/72 (83%)	190/360 (50%)	45/72 (62%)	33/69 (48%)	85/144 (59%)

5. BOARD APPLICATION

The board designed is very flexible and can be used for many applications, such as:

- Learning of programmable logic design
- Digital Logic Design application
- Robotics application
- ASIC prototyping
- System on Chip design
- Digital signal processing

6. CONCLUSION

In this paper, a prototype digital clock having two modes of display: binary coded decimal and seven segment displays with facility of reconfigurable CPLD controller is designed. Different issues related to interfacing of CPLD controller to other display devices also studied. This digital clock using CPLD having several advantages like reconfigurable controller, high frequency of operation, more number of inputs & outputs over conventional microcontroller. This can be easily modified according to future innovations as designed using small sub modules & reconfigurable controller.

7. REFERENCES

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