Improved Carry Select Adder with Reduced Area and Low Power Consumption

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ABSTRACT

Power dissipation is one of the most important design objectives in integrated circuits, after speed. As adders are the most widely used components in such circuits, design of efficient adder is of much concern for researchers. This paper presents performance analysis of different Fast Adders. The comparison is done on the basis of three performance parameters i.e. Area, Speed and Power consumption. We present a modified carry select adder designed in different stages. Results obtained from modified carry select adders are better in area and power consumption.

Categories and Subject Descriptors

VHDL, Behavioural modeling,

General Terms

Carry select adder, multiple stage adder

Keywords

Adder, Carry select Adder, carry skip adder, VHDL Simulation

1. INTRODUCTION

Addition usually impacts widely the overall performance of digital systems and a crucial arithmetic function. In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes adders come in to the picture. As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing multipliers. Due to device portability miniaturization of device should be high and power consumption should be low. Devices like Mobile, Laptops etc. require more battery backup. So, a VLSI designer has to optimize these three parameters in a design. These constraints are very difficult to achieve so depending on demand or application some compromise between constraints has to be made. Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry lookahead is the fastest one but consumes more area [2]. Carry select adders act as a compromise between the two adders. In 2002, a new concept of hybrid adders is presented to speed up addition process by Wang et al. that gives hybrid carry look-ahead/carry select adders design [7]. In 2008, low power multipliers based on new hybrid full adders is presented in [8]. In 2008, Hasan Krad et al provided the performance analysis for a 32-Bit Multiplier with a Carry look-ahead Adder and a 32-bit Multiplier with a Ripple Adder using VHDL and showed that CLA multiplier is almost double in speed as compared to RCA multiplier [9].

The rest of the paper is organized as follows. In section 2, a brief about ripple carry adder, carry skip and variable carry skip is given. In the same section carry select adder is introduced along with partitioning methodology. Also a new architecture with clock sharing is introduced. Section 3 provides the results obtained. Section 4 concludes the paper

2. FAST ADDERS

2.1 Ripple Carry Adder

Concatenating the N full adders forms N bit Ripple carry adder. In this carry out of previous full adder becomes the input carry for the next full adder. It calculates sum and carry according to the following equations. As carry ripples from one full adder to the other, it traverses longest critical path and exhibits worst-case delay. $S_i = A_i \text{ xor } B_i \text{ xor } C_i$

$C_i+1 = Ai\ Bi + (Ai + Bi)\ Ci$; where i = 0, 1, …, n-1

RCA is the slowest in all adders (O (n) time) but it is very compact in size (O (n) area). If the ripple carry adder is implemented by concatenating N full adders, the delay of such an adder is 2N gate delays from Cin to Cout. The delay of adder increases linearly with increase in number of bits. Block diagram of RCA is shown in figure 1.

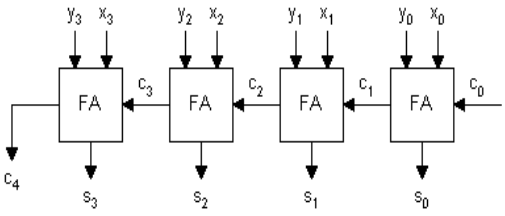

Figure1: Block diagram of RCA

2.2 Carry Skip Adder (CSKA)

A carry skip divides the words to be added in to groups of equal size of k-bits. Carry Propagate *pi* signals may be used within a group of bits to accelerate the carry propagation. If all the pi signals within the group are pi=1, carry bypasses the entire group as shown in figure 2.

$P = p_i * p_{i+1} * p_{i+2} * \ldots\ p_{i+k}$

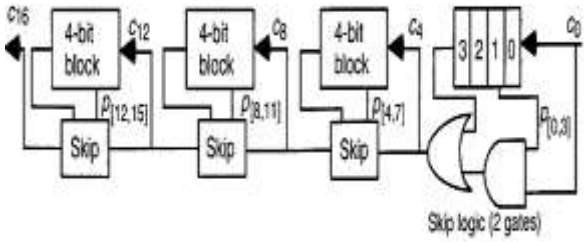

Figure 2: 16-bit Carry skip adder [6]

In this way delay is reduced as compared to ripple carry adder. The worst-case carry propagation delay in a N-bit carry skip adder with fixed block width *b*, assuming that one stage of ripple has the same delay as one skip, can be derived:

TCSKA = (b -1)+0.5+(N/b-2)+(b -1) = 2b + N/b – 3.5 Stages

Block width tremendously affects the latency of adder. Latency is directly proportional to block width. More number of blocks means block width is less, hence more delay. The idea behind Variable Block Adder (VBA) is to minimize the critical path delay in the carry chain of a carry skip adder, while allowing the groups to take different sizes. In case of carry skip adder, such condition will result in more number of skips between stages.

Such adder design is called variable block design, which is tremendously used to fasten the speed of adder. In the variable block carry skip adder design we divided a 32-bit adder in to 4 blocks or groups. The bit widths of groups are taken as; First block is of 4 bits, second is of 6 bits, third is 18 bit wide and the last group consist of most significant 4 bits.

Table 1 shows that the logic utilization of carry skip and variable carry skip 32-bit adder. The power and delay, which are obtained also given in the table1. From table it can be observed that variable block design consumes more area as gate count and number of LUT's consumed by variable block design is more than conventional carry skip adder.

2.3 Carry Select Adder (CSA)

The carry select adder comes in the category of conditional sum adder. Conditional sum adder works on some condition. Sum and carry are calculated by assuming input carry as 1 and 0 prior the input carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. The conventional carry select adder consists of k/2 bit adder for the lower half of the bits i.e. least significant bits and for the upper half i.e. most significant bits (MSB's) two k/ bit adders. In MSB adders one adder assumes carry input as one for performing addition and another assumes carry input as zero. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of output carry and sum. The selection is done by using a multiplexer. This technique of dividing adder in to stages increases the area utilization but addition operation fastens. The block diagram of conventional k bit adder is shown in figure 3.

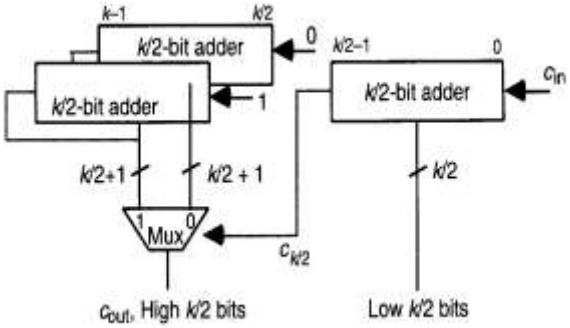

Figure 3: block diagram of k-bit adder [6]

2.4 Variable Stage Carry Select Adder

The idea of iterating the CSA in [10] will reduce the delay of the adder. The diagram of three-stage carry select adder is shown in figure 4. For constructing such a k-bit adder it is divided in to m

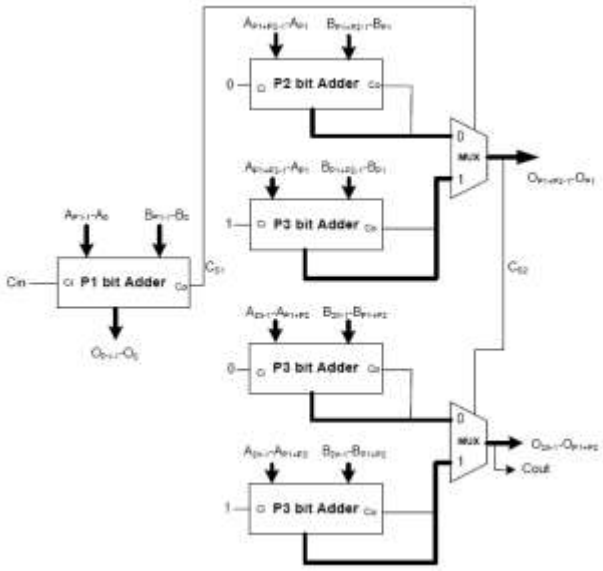

Figure 4: Three stage CSA [10]

groups where group i, contains P_i bits, such that bit width of the least significant part is P_1 and bit width of the most significant part is P_m. In part P_m adders will be duplicated or there are two adders; one computing addition for carry input 1 and another for carry input 0. Where cs1 is the carry out of P_1 bit adder. Cs2 is the carry propagated from the other part of adder. Cout is the final carry output of the adder. Similarly we can design for further 4 stage and 5 stage CSA adders to further reduce the delay. The main focus is on value of m. Some effort has been done to improve such adder s[1-4].

2.5 Clock Select Adder with Sharing (CSAS)

Instead of using two separate adders in conventional CSA, one for the Cs1 =1 and another for the Cs1=1 and another for the Cs1=0 [10]. One adder is used to reduce the area and power consumption. Each of the two additions is performed in one clock cycle. The block diagram of CSAS is shown in figure 5. This is a 32-bit adder in which least significant bit (LSB) adder is a ripple carry adder (RCA) adder, which is 22 bits wide. The upper half of the adder i.e. most significant part is 10 bits wide. This part works according to clock. Whenever clock goes high addition for the carry input one is performed. And when clock goes low then carry input is assumed as zero and addition is stored in adder itself. As can be seen from the figure 5 latch is used to store the sum and carry for Cin=1. Carry out from the previous stage i.e. least significant bit adder is used as control signal for multiplexer to select the final output carry and sum of the adder. If actual carry input is one then for computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry. Similarly, we can design CSAS adders of more stages to reduce area and power consumption.

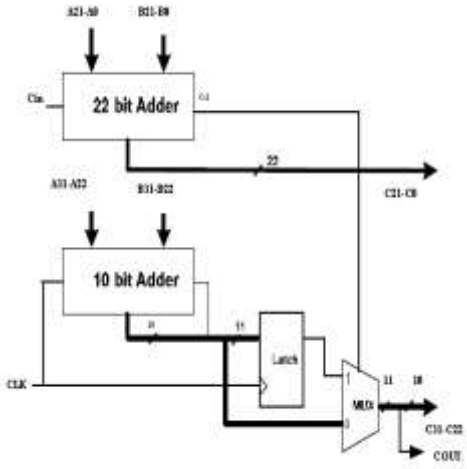

Figure 5: The architecture of CSAS [10]

3. SIMULATION RESULTS

Figure 6,7,8,9,10 and 11show the simulation results of 32-bit variable block carry skip adder, carry select adder, 3 stage carry select adder, 4 stage carry select adder, 2 stage CSAS and 5 stage CSAS respectively.

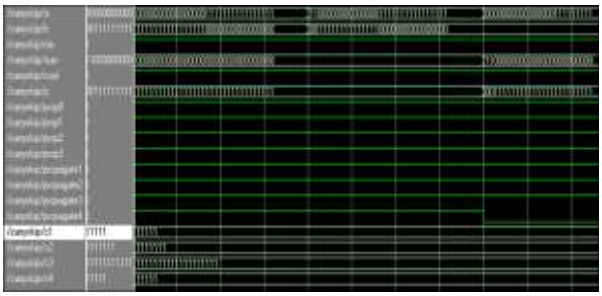

Figure 6: Simulation waveform of variable carry skip adder

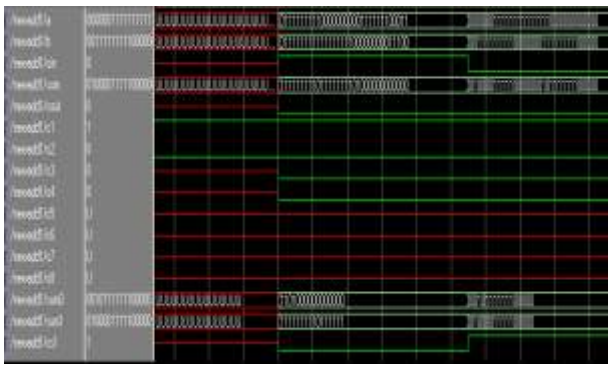

Figure 7: Simulation waveform of carry select adder

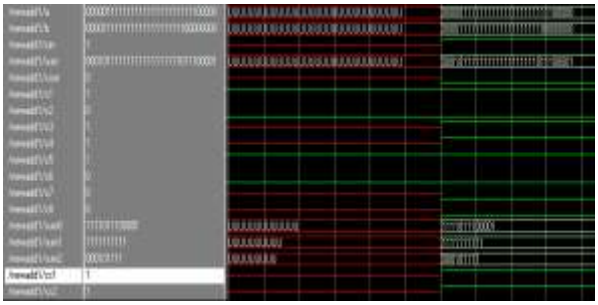

Figure 8: Simulation waveform of 3 stage carry select adder

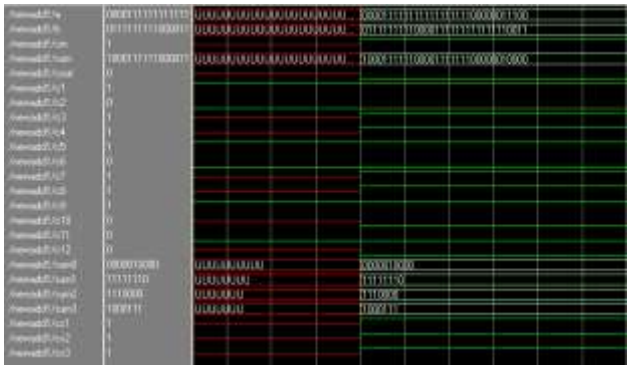

Figure 9: Simulation waveform of 4 stage carry select adder

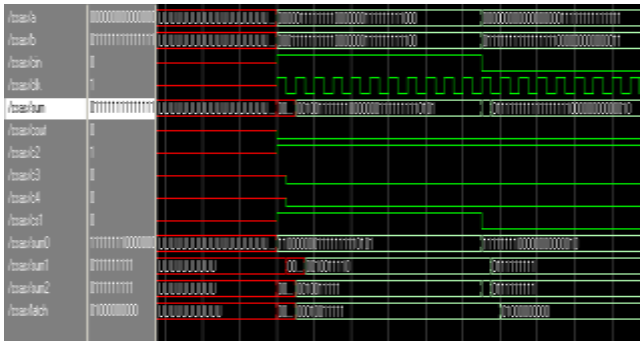

Figure 10: Simulation waveform of CSAS

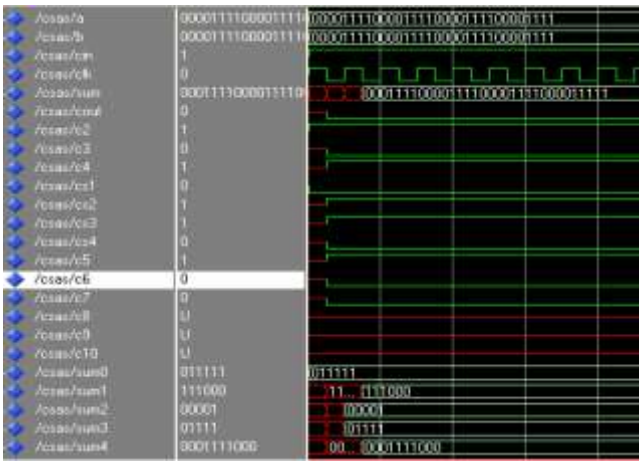

Figure 11: Simulation waveform of 5 stage CSAS

Table1 shows the comparison of 32-bit carry skip adder and 32-bit variable carry skip adder. Table2 represents the comparison of area, power and delay of ripple carry, carry select, 3 stage and 4 stage carry select adders. Table 3 provides the results obtained after design and implementation of 2 stage CSAS and 5 stage CSAS

Table1. Carry Skip and Variable Block Carry Skip design comparison for area, delay and power

	Carry skip	Variable carry skip
LUT's	51/7168	65/7168
Bonded IOB's	98/173	98/173
Gate Count	348	390
Delay (ns)	29.082	26.054
Dynamic Power (mw)	72.06	72.13

4. CONCLUSION

All the adders designed are 32-bits wide. CSAS 5 stage consists of 5 stages with each block from LSB block to MSB blocks are [6-6-5-5-10] bits wide. These adders are faster than ripple carry adders but slower than carry select adders. All the adders are designed using VHDL (Very High Speed Integration Hardware Description Language), Xilinx Project Navigator 9.1i is used as a synthesis tool and ModelSim XE III 6.2g for simulation. FPGA Spartan3 is used for implementing the designs.

Gate count reduction is a sign of area reduction. Gate count of csas 2 stage is 11 less than carry select, 80 less than 3 stage carry select and 110 than 4 stage carry select adder. For further to

Table 2: Comparison of ripple carry, carry select, 3 stage and 4 stage carry select adders

	Ripple carry adder	Carry select	3 stage carry select	4 stage carry select
LUT's	65	82	91	94
IOB's	98	98	98	98
Gate Count	390	492	564	591
Delay (ns)	55.634	39.967	37.94	37.033
Dynamic power (mw)	72.01	57.66	57.32	56.91

Table3. Comparison of CSAS 2 stage and CSAS 5 stage

	CSAS 2 stage	CSAS 5 stage
LUT's	99/7168	118
IOB's	99/173	99/173
Gate Count	481	1,191
Delay (ns)	43.707	24.497
Dynamic Power (mw)	48.94	15.83

explore in this work is to design the adder in a way to reduce the delay as the area and power reduces. Wherever there is need of smaller area and low power consumption, while some increase in delay is tolerated, such designs can be used. These adders are faster than RCA and slower than CSA.

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