

Fault Tolerant Irregular Modified Alpha Network and Evaluation of Performance Parameters

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ABSTRACT

Interconnection Networks are playing a vital role in parallel processing. The speed of hardware has become proportional to response time of electronic circuits. But requirement for more reliability, bandwidth, processing power and throughput is increasing constantly.

This paper introduces a new Multistage Interconnection network named as irregular Modified Alpha Network (Modified ALN), which is a modified form of Alpha network. This network acquires increased values of performance parameters as compared to other existing MINs like Alpha, Quad Tree and Augmented Shuffle Exchange Network.

KEY WORDS

Multistage Interconnection Network, design of new Network, Redundancy Graph, Routing, Fault Tolerance, permutation passable, Experiment results, Bandwidth, Probability of Acceptance, Processor Utilization, Processing Power, Throughput, Conclusion.

1. INTRODUCTION

A new class of irregular Interconnection Network has been proposed and analyzed. The Interconnection Network connects Processors and /or Memory Modules. The new Network has lesser no of stages as compared to Alpha Network [7] maintaining the full access capability at the same time. Thus the Network has low latency [1], low cost and attains higher values of other important parameters.

2. DESIGN OF MODIFIED ALPHA NETWORK

The Network is an Irregular Multistage Interconnection Network, of size $N \times N$. It has N sources and N destinations. The MIN consists of n stages ($n = \log_2 N$). The network Comprises of two identical groups of switching elements (SEs), named as G_0 and G_1 . Each group incorporates $N/2$ sources and $N/2$ destinations. Both the groups are connected to the N inputs through N multiplexers, and to the N outputs through N no. of demultiplexers. The switches in all the stages are of size 3×3 except the last one. The switches in the stages $n-3, n-2$ and $n-1$ have been connected to each other through links called as auxiliary

links. These links are used when the SE in the next stage is busy or faulty. This makes the network more fault tolerant and reliable.

The modified Alpha network of size $2^n \times 2^n$ consists of $(2m-2)$ stages where $m = \log_2(N/2)$. This network has 2^n no. of switches of size 3×3 and 2^{n-1} no. of switches of size 2×2 . Each source is connected to one switching element in each group with the help of multiplexers. The network of size 16×16 is depicted in following figure 1

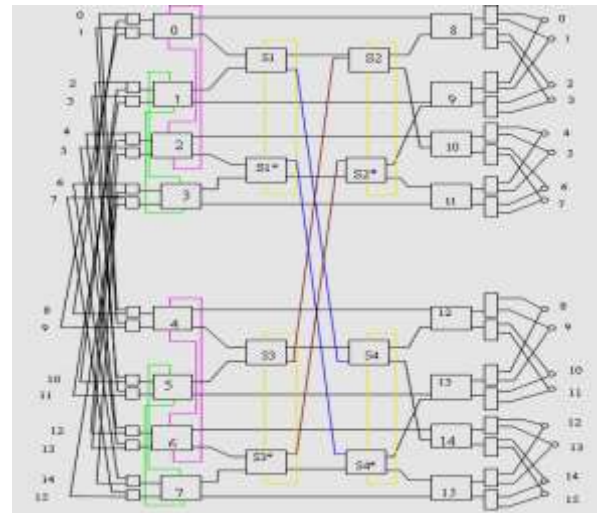


Figure 1
16 * 16 Modified Alpha Network

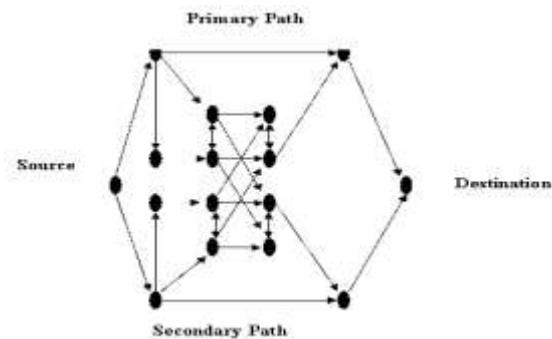


Figure 2
Redundancy Graph

The redundancy graph is the pictorial representation of all the paths available from all sources to all destinations. Figure 2 shows all the paths available in proposed Modified Alpha Network.

3. ROUTING ALGORITHM FOR MODIFIED ALPHA NETWORK

Let the source and destination in binary [11] be represented as

$S = S_{n-1} \dots S_1 S_0$

$D = D_{n-1} \dots D_1 D_0$

Step1 : Start

Step2 : The MSB of the destination address is checked and on the basis of it ,one of the sub networks G0 or G1 is selected.

Step3 : Let us suppose the address of the following SE is known. If the destination address is the address of this SE ,then the shortest path is used and the further routing is not required as the data has reached the destination.

Step4 : If the SE is busy then route the data to auxiliary SE through auxiliary links. If this is also busy then drop the request. Otherwise go to step 5 .

Step5 : The secondary path is selected .Set MSB of the routing tag as 1.The bits of the destination will make the data to reach the destination through intermediate stages. If the SE in any of the stages except the last one , is busy go to step 5

Step6 : Route the data [6] to auxiliary switch in the same stage (Route the data to auxiliary switch in the previous stage in case of faulty SE)

Step7 : Bit D0 of the routing tag will guide the data through a particular demultiplexer and the destination will be reached.

Step8 : Stop

Sample : Routing example from source 0000 to all destinations for the Modified Alpha Network

The table 1 gives the information of path lengths available from source 0000 to all the destinations in the network.

Table 1 All Path Lengths available

Source	Destination	Path Lengths Available
	0000	2,4
	0001	2,4
	0010	2,4
	0011	2,4
	0100	4
	0101	4
	0110	4
	0111	4
0000		
	1000	2,4
	1001	2,4
	1010	2,4
	1011	2,4
	1100	4
	1101	4
	1110	4

The table 2 proves that proposed network has lesser shortest and longest path lengths between source and destination.

Table 2 Comparison of Path Lengths available

Network	Path Lengths
Alpha	$\log_2(N)-2, \log_2(N)+1$
Modified Alpha	$\log_2(N)-2, \log_2(N)$

4. FAULT TOLERANCE AND REPAIR

If the network is able to work, of course with degraded efficiency, in the presence of faults in critical components [4] then the network is called as fault tolerant. A network is single fault tolerant if it can work with full access in the presence of fault in single SE. If the network is able to provide connections from all sources to all destinations in the presence of k faults in the network [8] , then this network is called as k fault tolerant network.

The proposed MIN satisfies the fault tolerant criteria [10] [12] because it can work in the presence of certain faults. If there is fault in the primary path then secondary path will be chosen for routing the data.

Moreover the auxiliary links [2] in all the stages except the last one provides the alternate route of the data. The critical case is when the fault is present in the SE in same loop. In this case certain pair of source and destination shall be disconnected.

Theorem 1 : Modified Alpha Network is single switch fault tolerant in all the stages

Proof: The auxiliary links are available in all the SE in all the stages except the last one. If fault in any of these SE happens then the data will be routed to the auxiliary SE in the same stage through auxiliary links.

Theorem 2 : Modified Alpha Network will be able to work in the presence of faults in the SEs in the loop in one Group at a time.

Proof : By guiding the data from the other Group (fault free) to the same stage ,where the fault was present in the faulty Group, we can pass the request to the desired destination.

Lemma 1 : If all the SEs in the loops in both the groups are faulty then Modified Alpha network fails.

Repair : To rectify just replace the loop engaged in the faulty components.

5. EXPERIMENTAL RESULTS ON PERFORMANCE PARAMETERS

The Modified Alpha Network has been analyzed[7][15]on the basis of following parameters.

5.1 Bandwidth(BW)

It is defined as average number of active memory modules in a transfer cycle of the Interconnection Networks. The bandwidth of $a^n * b^n$ (a^n no of sources and b^n no of destinations) Network is calculated as

Bandwidth = $b^n * P_n$, where P_n is the probability of requests being forwarded. & $P_0 = P$

The equations derived for Modified Alpha Network are

$$\begin{aligned} P[1] &= 1 - (1 - P[0]/3)^3 \\ P[2] &= 1 - (1 - P[1]/6)^3 \\ P[3] &= 1 - (1 - P[2]/3)^3 \\ P[4] &= 1 - \{(1 - P[3]) * (1 - P[1]/2)\}^2 \end{aligned}$$

The probability of forwarding the requests from switches of first stage to second stage is half and switches are of size $3*3$. The same no of switches have been used in the third stage so the probability of requests is same. The final stage is getting the requests from first as well as third stage.

5.2 Probability Of Acceptance (Pa)

It is defined as ratio of bandwidth to the expected no of requests generated per cycle.

$$Pa = BW / a^n * p \text{ req gen}$$

5.3 Processor Utilization

It is defined as percentage of time the processor is active doing computation without accessing the global memory.

$PU = BW / a^n * p \text{ req gen} * T$, where T is average time used for a memory or read/write operation.

5.4 Processing Power

It is defined as sum of processor utilization over the number of processors.

$$PP = a^n * PU$$

5.5 Throughput

It is defined as maximum amount of data delivered per unit time

$$\text{Throughput} = PU * p \text{ req gen}$$

After simulating the above formulas on simulator designed in c#, the values of performance parameters for Modified Alpha Network have been shown in following table 3.

Table 3

Performance Parameters of Modified Alpha Network

Req. gen	Bandwidth	Probability of acceptance	Processor Utilization	Processing Power	Throughput
0.1	2.83494	1.77183	0.50623	8.09968	0.05062
0.2	5.06096	1.58155	0.45187	7.22992	0.09037
0.3	6.82314	1.42148	0.40613	6.49808	0.12183
0.4	8.22834	1.28567	0.36733	5.87728	0.14693
0.5	9.35648	1.16956	0.33416	5.34656	0.16708
0.6	10.26818	1.06960	0.30560	4.88960	0.18336
0.7	11.00896	0.98294	0.28084	4.49344	0.19658
0.8	11.62480	0.90818	0.25948	4.15168	0.20758
0.9	12.11310	0.84118	0.24033	3.84528	0.21629
1.0	12.52368	0.78273	0.22363	3.57808	0.22363

6. COST ANALYSIS

The cost of a network is calculated by considering the complexities of the components used. For a switch the cost is proportional to the no of gates counts i.e. no of cross points within a switch. The cost of multiplexers and demultiplexers is calculated in the same way. For example $n:1$ multiplexer has n units of cost and $1:n$ demultiplexer has same units of cost i.e. n units of cost.

The cost of Modified Alpha Network is calculated as

- Total no of $3*3$ switching elements = 16, cost = 144
- Total no of $2*2$ switching elements = 08, cost = 32
- Total no of $2:1$ Multiplexers = 16, cost = 32
- Total no of $1:2$ Demultiplexers = 16, cost = 32

Total cost of the network is 240 units.

The table 4 describes the cost function of Alpha and Modified Alpha Network.

Table 4
Cost effectiveness

Network	Cost Function
Alpha	$N/2[9 \log_2(N/2) + 7.5]$
Modified Alpha	$N/2[9 \log_2(N/2) + 3]$

The figure 3 shows the comparison of Bandwidth of Modified Alpha Network against the other popular networks.

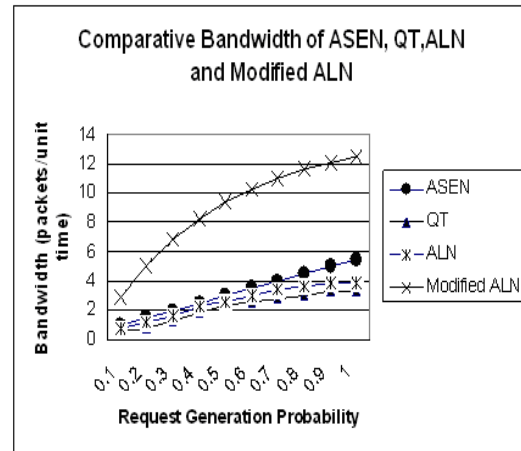


Figure 3

The figure 4,5,6 and figure 7 show that the performance parameters of Modified Alpha Network are better as compared to other discussed Networks.

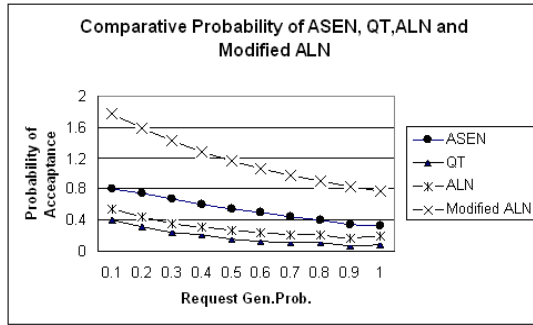


Figure 4

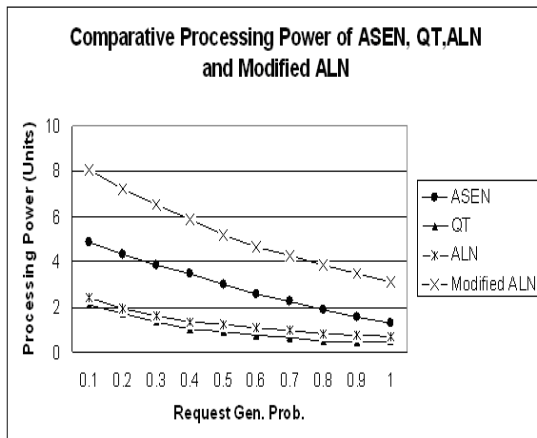
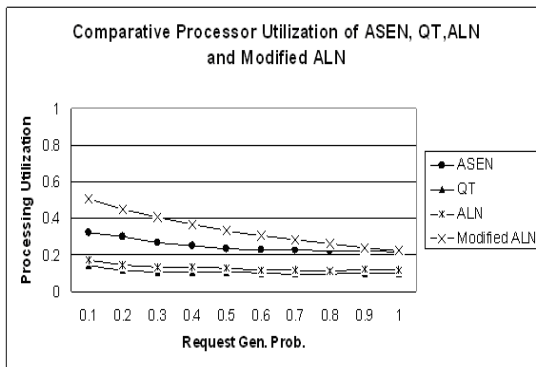


Figure 6.

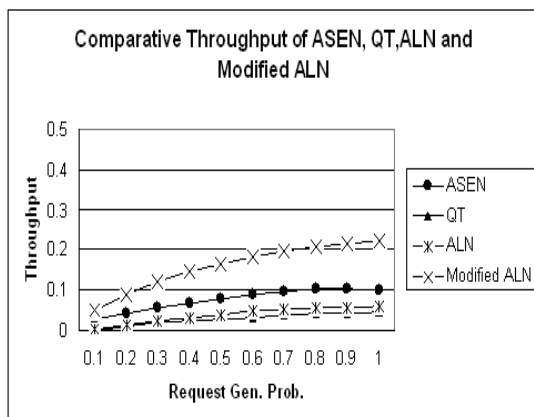


Figure 7

The figure 8 compares the cost of the different networks discussed in this paper. It is clear that the cost of Modified Alpha Network is less as compared to other networks as discussed. The cost is same for Augmented Shuffle Exchange Network.

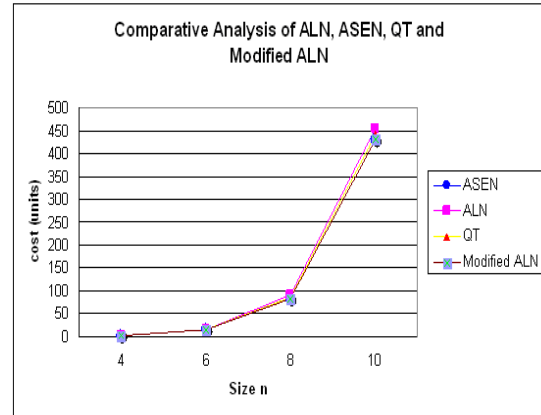


Figure 8

CONCLUSION

The proposed Fault Tolerant Irregular Modified Alpha Network is better as compared to the other discussed Networks. It has more bandwidth, probability of acceptance, processor utilization, processor power and throughput than Alpha, Quad tree and Augmented Shuffle exchange Networks.

The proposed network has reduced the latency by reducing the stage in the Alpha network. Hence the maximum path lengths have also been reduced. Moreover the cost of the proposed network is less as compared to Alpha and Quad tree and the cost is same for Augmented Shuffle Exchange Network.

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