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Optimization of Chip Interconnect Area by using Interconnect Length and Width

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ABSTRACT

This paper presents methodologies that provide better correlation between the apriori and posteriori estimation of interconnect length, width, area and power. A method to generate random realistic benchmark circuits for analysis is implemented. A prediction model that predicts the length, width, area and power of the benchmark circuit is developed. The net list is passed through the placement and routing phases to obtain the actual length. From the estimated length, the width, area and power are estimated. The effectiveness of the prediction technique used is validated from the results obtained. We postulate that the predicted area which comes out with a smaller error percentage than predicted length can be used as a termination condition in Simulated Annealing for placement. Results are compared for proving optimization with Lagrange's Method.

Keywords- VLSI, DSM,FPGA

I Introduction

With the advancement of integrated technology from MSI through LSI towards VLSI, the minimization of the chip area became the most critical issue. This involves

- Component size reduction
- Interconnect area minimization
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With the advent of the DSM era, considerable component size reduction has already been achieved. However there has not been an equivalent reduction in interconnect length and width and consequently interconnect dominance has been observed. So, considerable efforts are now being taken towards interconnect area minimization too. As technology pushes forward, chip component sizes continue to decrease, but the complexity of the circuits to be implemented on the chips is increasing by the day. As a consequence, the length of semi global and global wires increases relative to the feature size and the relative cost of interconnect in the cost of VLSI chips is becoming ever more important.

Interconnect dominance causes large problem for designers; because most interconnect properties relate to their geometries and only become known during physical design. Hence they are very difficult to optimize before at least some part of the physical design has been executed. So interconnect prediction is gaining more and more importance. Moreover, as VLSI technology shrinks to DSM geometries, the parasitic due to interconnect is becoming a limiting factor in determining circuit performance. Hence interconnect prediction is very important for early feasibility studies in design flows, evaluation of new computer architectures and exploration to future systems. There is considerably less work done on the prediction of the width and hence the total interconnect area

A method to generate random realistic benchmark circuits for analysis is implemented. A prediction model that predicts the length, width, area and power of the benchmark circuit is developed. The net list is passed through the placement and routing phases to obtain the actual length. From the estimated length, the width, area and power are estimated and validated. The predicted values are then used as a termination condition in Simulated Annealing.

The circuit is modeled as a set of modules with varied area. To best emulate a full custom design realistic circuit nets are generated randomly connecting pins from various modules and the lengths of their segments are also generated randomly in a normal distribution. The frequency of occurrence of each of the segment lengths is found from which the probability distribution for segment length is obtained. From the segment lengths and their corresponding probabilities thus obtained, an expected value of interconnect length is predicted. The interconnect width is predicted based on the predicted value of the interconnect length. The predicted interconnect area is determined from the already predicted interconnect length and width. We also predict the power that the design is expected to consume. The prediction model used predicts for internal nets only.

II Generation of benchmark circuits:

The circuit level netlist generation is a computer-performed method for generating a circuit level netlist from a logic design of an application specific integrated circuit [1] .A number of approaches to benchmark netlist generation were presented in [2], [3], [4], [5], [6], and [7]. Generating random benchmark circuits for routability measurement was first done by Darnauer et al [3]. Development of CIRC tool which emphasizes on the essential heuristics of the different types of circuits is stated in [3] and [4]. Then a tool GEN was applied to generate random circuits parameterized by those heuristics. Pistorius et al. [5] presented another tool, PartGen, to generate netlists for partitioning to multiple FPGAs. Tool gnl [6] is based on a bottom-up clustering approach according to Rent's rule [8]. At last, [7] reviewed existing benchmark generation methods and discussed the advantages and drawbacks of different methods through direct validation.

Most of the above methods were designed for partitioning and routability measurement of FPGAs. Circuits generated by them lack module area information, which is the most important information for floor planning tools. Furthermore, some input metrics from the above generator tools are unnecessary for floor planning. In our approach, we used floor planning benchmarks with a larger number of modules and nets, and with information about power dissipation [9]. Since the generation of nets is done by taking into account the size of the modules, the netlist though generated randomly resembles a realistic circuit [6].

While developing the netlist these were some of the heuristics that were kept in the mind that helped us obtain a realistic circuit. Some of them are as follows.

- There cannot be a few small modules or few very large modules.
- The number of pins on a module cannot exceed that it cannot fit within the length of the module.
- There has to be a good proportion of input and output terminals.

Thus giving only the number of modules, ratio of internal nets to external nets, Rent's exponent, average number of pins per module as the input, we obtain a realistic set of netlists [9]. After generating the module sizes, the net degree distribution is obtained from which the netlists are generated for the required number of modules.

III .Prediction Techniques:

A) Length Prediction:

One of the predominant techniques available for length prediction is the Donath's technique. A formula for an upper bound on expected average interconnection length, based on partitioning results, is given for linear and square arrays of gates [10] .This upper bound gives significantly lower interconnection length than the bound based upon random placement. Hence, in its original form, Donath's technique was heavily constrained by the underlying circuit and architecture models. [11] shows how a careful relaxation of those constraints results in very high correlations between predicted and experimentally measured average wire lengths and provides a much improved accuracy in predicting wire length distributions. Many researchers have observed that different placement algorithms produce different individual wire lengths. To obtain accurate results, individual wire-length prediction should be coupled with the placement flow [12]. Hence [10] and [11] cannot be used for reasons cited above. So, analytical and numerical extensions to this model to overcome some of these constraints have also been proposed [13]. A new concept for wire-length prediction, the semi-individual wire-length prediction, has also been proposed [14]. Structural metrics, such as mutual contraction and net range, are used to predict where interconnects have a tendency to be long or short in the final layout. The very good correlation of the prelayout measures with the post layout interconnect lengths is demonstrated in [12]. The probabilistic method for length prediction [15] brings out better correlation and the prelayout wire-length-prediction technique can be applied in logic synthesis, targeting wiring cost, and congestion minimization.

In probabilistic approach [15], the nets are modeled as a tree in a hierarchical fashion. The tree is composed of segments where each segment is assumed as a connection between two modules. Taking the segment lengths as independent random variables, a normal distribution of these segment lengths is found out since normal distribution is an approximation of any other distribution. The tree levels are then generated in a uniform fashion. To find the normal distribution two parameters are essential namely mean and standard deviation. The mean is the average of the largest and the smallest possible values while the standard deviation is obtained by finding the variability or dispersion of the given data set. Depending on the level of the tree, segments are to be generated for the net. Greater the level of the tree, greater will be the number of segments in the net. The length of each of the segments of the net will be generated randomly according to a normal distribution

Once such segments are generated for every net, they are stored in the array Li. For every length value in Li, the number of segments having that length is correspondingly stored in an array Fi (i.e) the frequency array. From Fi, an array Pi is generated which consists of the ratio of the corresponding frequency in Fi to the total number of segments generated for the netlist.

Expected length of every segment is obtained as follows.

Expected Length = $\sum li*pi$

Where,

li = segment length.

pi = probability of obtaining that length.

Probability of a particular value li is taken to be a ratio of the frequency of

That value by the total number of segment lengths. Hence, frequency distribution is taken to obtain pi. Hence, expected length is the predicted length of a segment.

B) Apriori estimation of Width:

We use a novel methodology optimizing global interconnect width and spacing for International Technology Road map for Semiconductors technology nodes[16]. For a given technology, repeater insertion and interconnect width are two key solutions to reduce the delay of a long interconnect. Using fat wires which reduce delay, however, may reduce global interconnect bandwidth. In [20], interconnect width and spacing are simultaneously optimized for bandwidth, but no analytical expression for the optimal width and spacing is given, and the global interconnect delay is also not considered. For achieving large bandwidth and short latency simultaneously, the product of delay and bandwidth has been introduced as a figure of merit [21].However, the interconnect width, spacing, thickness and dielectric height are assumed to be equal and able to be arbitrarily varied in [21], which is not realistic because for a given technology and a given layer, the interconnect thickness and dielectric height cannot be changed. In fact, only the interconnect width and spacing can be changed if their values are not less than the given minimum value of a technology. The methodology optimizing global interconnects width only cannot optimize the spacing of global interconnects because it regards the line spacing for two extreme scenarios: line spacing kept constant at its minimum value and line spacing kept the same as line width. These two extreme scenarios cannot maximize the figure of merit.

The effects of global interconnect width and spacing on performance, such as delay, bandwidth, repeater area and power dissipation, are analyzed. The trade-off between delay and bandwidth is needed for the whole performance and the product of delay and bandwidth is used as the figure of merit for simultaneous short latency and large bandwidth.

The formula for obtaining the delay for interconnects with buffer insertion is shown. Formula (1) shows the time constant of a segment and (2) shows the total delay.As we can see the delay per unit section is given with k denoting the optimum repeater size and h the length of the segment.

$$\tau = r_s(c_0 + c_p) + \frac{r_s}{k}ch + rhkc_0 + \frac{1}{2}rch^2 \tag{1}$$

$$\text{delay} = \frac{L}{h} \times \tau \log 2 \propto \frac{\tau}{h} \tag{2}$$

Thus the optimum delay per unit length (with repeaters inserted) is given by:

$$\frac{\tau}{h} = \frac{1}{h}r_s(c_0 + c_p) + \frac{r_s}{k}c + rkc_0 + \frac{1}{2}rch.$$

However, since we consider only interconnects of length L with no repeaters we obtain the delay as the product of the delay per unit section and the length of the interconnect. The delay of global interconnects with the driver resistance Rs, the input capacitance C0 and the output capacitance Cp is given by

$$\begin{aligned} D &= \log 2 \cdot \left[R_s(C_0 + C_p) + R_s cL + C_0 rL + \frac{1}{2}rcL^2\right] \\ &= \log 2 \cdot \Big[R_s(C_0 + C_p) + R_s\left(c_a + c_b W + \frac{c_c}{S}\right)L \\ &\qquad + C_0\frac{\rho}{WT}L + \frac{L^2}{2}\frac{\rho}{WT}\left(c_a + c_b W + \frac{c_c}{S}\right)\Big] \end{aligned}$$

The delay of global interconnects decreases as interconnect spacing increases. By setting $\partial D/\partial W = 0$, the optimal width for the minimum delay is given by [16]

Thus we find that the optimized width can be calculated for any

$$W_{\text{opt}} = \sqrt{\frac{\rho}{TR_s c_b}\left(C_0 + \frac{c_a L}{2} + \frac{Lc_c}{2S}\right)}$$

given length and a given technology.

C) Area Prediction:

From the predicted length and width values, the cross-sectional area of the interconnects is found which is thus the product of the interconnect length and the interconnect width.

D) Power Prediction:

The power consumption of global interconnects is found to be proportional to interconnect capacitance per unit length, the energy dissipation and the clock frequency in addition to its dependence on the interconnect length and width values. From the value of interconnect length predicted (L), the average power consumed by an interconnect can be predicted. The average power consumption of an interconnect is given by

Where

Echip -the chip width for global interconnects
W - interconnect width
S - the interconnect spacing
C0 - input capacitance
Cp - output capacitance
c(W,S) - interconnect capacitance per unit length
L - average interconnect length
Vdd - power supply voltage

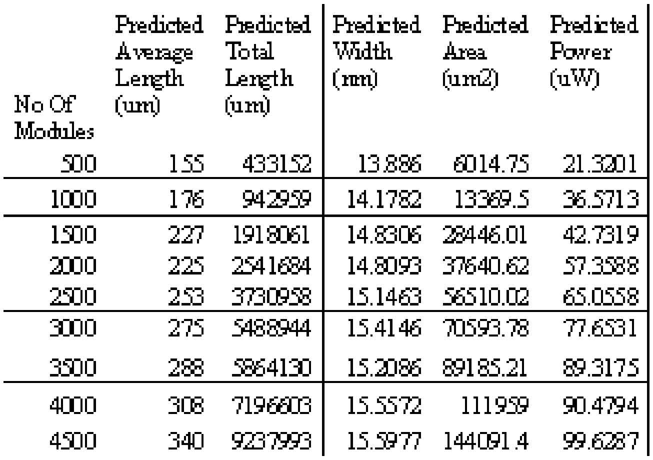
f - clock frequency

The power consumption of global interconnects decreases when interconnect width and spacing increase. So, the greater the interconnect width, the greater the power consumption.

$$P = \frac{E_{\text{chip}}}{(W+S)}\left(C_0 + C_p + c(W,S)L\right)V_{dd}^2 f$$

III .Results and Analysis:

Table 1: Predicted length, width, Area and power



No Of Modules	Predicted Average Length (um)	Predicted Total Length (um)	Predicted Width (nm)	Predicted Area (um2)	Predicted Power (uW)
500	155	433152	13.886	6014.75	21.3201
1000	176	942959	14.1782	13369.5	36.5713
1500	227	1918061	14.8306	28446.01	42.7319
2000	225	2541684	14.8093	37640.62	57.3588
2500	253	3730958	15.1463	56510.02	65.0558
3000	275	5488944	15.4146	70593.78	77.6531
3500	288	5864130	15.2086	89185.21	89.3175
4000	308	7196603	15.5572	111959	90.4794
4500	340	9237993	15.5977	144091.4	99.6287

On making a comparison with the apriori and posteriori techniques for length, width, area and power, the following results are obtained.

Varying only the number of modules present, we predict the values for length, width, area and power

using the techniques described above. From the graph we find that there is an increasing trend in the average net length. However, this need not be strictly so. The average net length in addition to its dependence on the module size depends on the distribution of net degree also. The predicted values for the total wire length also show an increasing trend. This is because with increasing modules, the length also increases[18].Thus ,the length is directly proportional to the number of modules.

The width, in addition to its dependence on technological parameters depends on the length also [16] that is; the width is in direct proportion to the average net length. Although the width is found to increase in our analysis, it may not be the case always for the same reasons stated above. The predicted values for power and area depend on the length and the width and hence increase for higher module sizes.

A comparison is also made with the estimated values to determine the level of correlation. The posteriori estimation values are

Table 2: Estimated length, width, Area and power

No Of Modules	Estimated Average Length (um)	Estimated Total Length (um)	Estimated Width (nm)	Estimated Area (um2)	Estimated Power (uW)
500	104	288084	14.061	4052.35	20.82
1000	144	765448	14.937	11433.2	34.6008
1500	185	1557294	15.179	23637.5	40.1328
2000	200	2123859	15.771	33496.2	49.4719
2500	243	3263062	16.076	52456	51.541
3000	245	4196550	16.236	68136.4	61.4733
3500	258	5124969	16.898	86602.8	70.2678
4000	285	6338498	17.071	108204	71.1148
4500	292	8075584	17.621	142300	79.0327

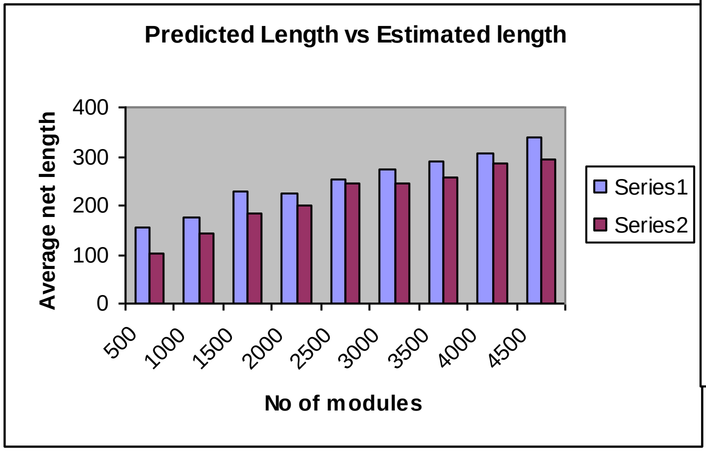


Fig1 Predicted interconnect length vs Estimated length

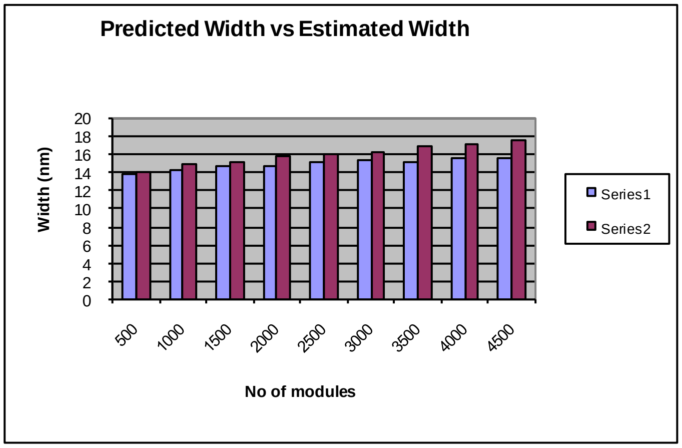


Fig2 Predicted interconnect width vs Estimated width

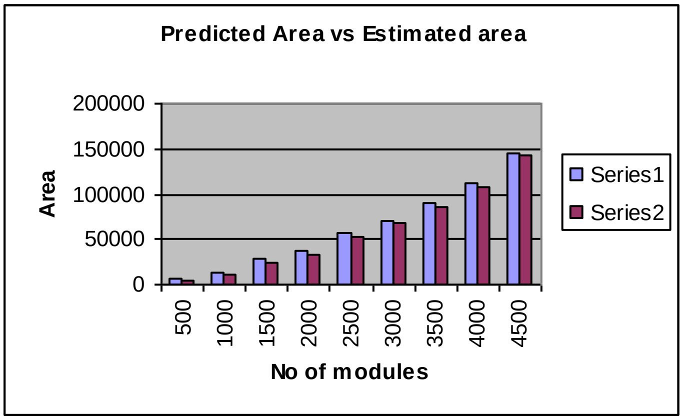


Fig3 Predicted interconnect Area vs Estimated Area

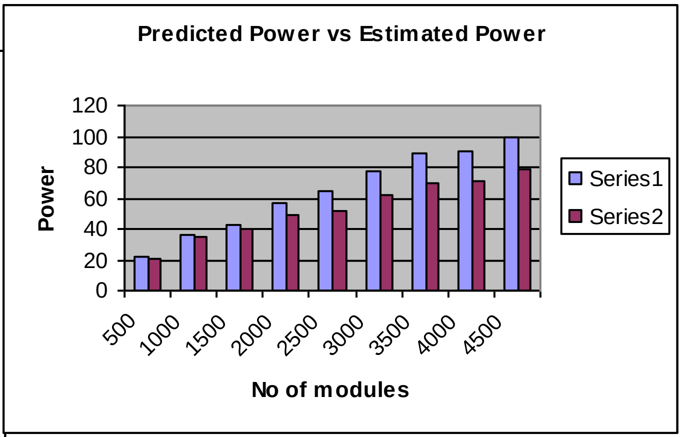


Fig4 Predicted interconnect power vs Estimated power

The error rate of the predicted length is observed to be lesser for greater values of the number of modules. Hence the length prediction technique used is deemed to be better suited for realistic circuits which generally possess greater number of modules. The predicted values of the interconnect area show a strictly decreasing trend and hence is found to be more accurate for greater number of modules and hence is realistic. The error rate for the predicted value of width initially shows an increase and then stabilizes as the value of the no. of modules gets higher. The error rates in the predicted values of power also show a trend similar to that observed for the predicted width values and hence is optimum for larger circuits.

Table 3: Error percentage in length, width, Area and power

No Of Modules	Error in length (%)	Error in width (%)	Error in Area (%)	Error in Power (%)
500	49.038	1.241767777	48.43	2.402
1000	22.222	5.077460734	16.94	5.695
1500	22.703	2.292701567	20.34	6.476
2000	12.5	6.10028279	12.37	15.94
2500	4.1152	5.781396767	7.728	26.22
3000	12.245	5.060882098	3.606	26.32
3500	11.628	9.998698086	2.982	27.11
4000	8.0702	8.867136472	3.47	27.23
4500	16.438	11.48232223	1.259	26.06

IV RESULTS COMPARISON WITH STANDARD MODEL

Comparison of probabilistic based approach with Lagrange's based [23] algorithm. Table 4

Table 4 Lagrange's Vs Probabilistic models

	Lagrangaes based Algorithm		Probabilistic Approach	
No	Area		Area	
	Init(kUm2)	Fin(kum2)	Init(kUm2)	Fin(kum2)
500	766.96	153.59	60.1475	40.52
1000	1312.47	262.75	133.695	114.33
1500	1670.75	354.48	284.46	236.37
2000	1915.59	383.49	376.4	334.96
2500	2696.96	539	565.1	524.56
3000	3737.55	748.19	705.93	681.36
4500	5291.24	1059.24	1440.91	1423

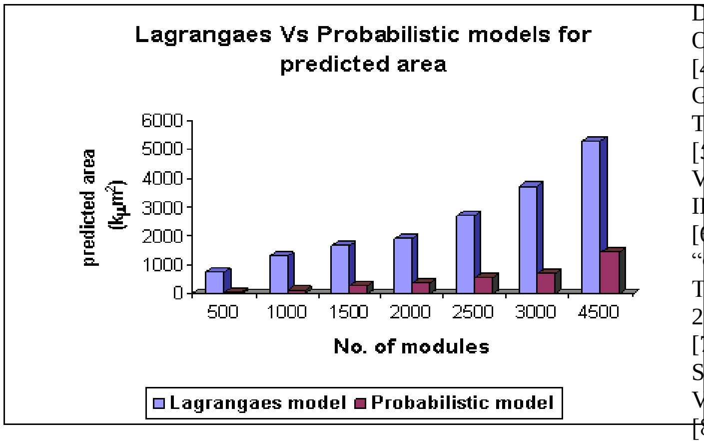


Fig 5 Probabilistic vs Lagrangaes models for predicted area

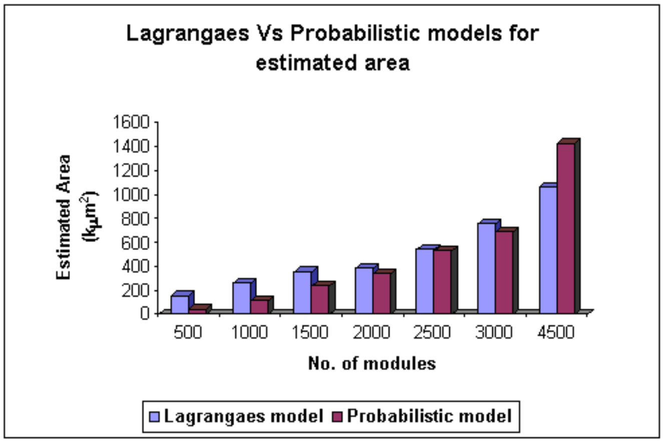


Fig 6 Probabilistic vs Lagrangaes models for estimated area

V CONCLUSION:

The prediction model is for a full custom design assuming no circuit model or architectural model. the predictions have been validated with estimation and the prediction model gives only an average error rate of 15.12% for length, 10.97% for width, 8.91 % for area and 20.13 % for power. As the technology dictates, prediction accuracy of 80% is considered extremely efficient. Till now simulated annealing algorithms used for placement and routing optimization have used the predicted value of interconnect length as a termination condition. . With nearly 91% accuracy in area prediction, as compared to the 84% accuracy in length prediction, our idea of using area as the termination condition (instead of length) in Simulated Annealing is justified This method thus gives more optimized results for placement and routing when compared to standard Langrangaes Methos[23].

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