Design of COFDM Transceiver Using VHDL

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ABSTRACT
OFDM is combined with channel coding scheme i.e. FEC (Forward Error Correction) called CODED OFDM or COFDM is especially suitable for high speed environment because it provides data transfer at higher speed with reliable transmission. Main focus of this paper is to design COFDM transceiver which operates with FEC, scrambling, block interleaver with conventional OFDM system to overcome the problem in wireless link i.e. ISI, ICI, fading etc. In this paper, COFDM transceiver designing details and simulation results are discussed after that COFDM modulator is compared with previous work which ensures present work is better than previous work. COFDM Transceiver is designed and synthesized using Xilinx Project Navigator XILINX ISE 9.1i and simulated using ModelSim 5.8c simulator.

General Terms
Digital System Design, Wireless Communication, Data and information system

Keywords
OFDM, COFDM, FEC, Convolution Encoder, Viterbi Decoder

1. INTRODUCTION
In the field of wireless communication OFDM (Orthogonal Frequency Division Multiplexing) is the suitable candidate to overcome the problems like multi-path fading, ISI (Inter Symbol Interference), ICI (Inter Carrier Interference), low bit rate capacity, need higher power to transfer the data etc [3] [4]. With increasing data transfer rate, it is very important that data must be transmitted with carefully and reliable transmission should be take place in wireless link. So OFDM is combined with suitable channel coding scheme to perform reliable transmission, when OFDM is combined with channel coding scheme then it is called CODED OFDM or COFDM [3]. Coding scheme must be chosen for any system which satisfies requirements of high data rate as well as good error capability and according to complexity, suitable delay and desired coding gain for system.

The aim of this work to show the compatibility of designing and implementing a COFDM transceiver on FPGA. In this work COFDM transmitter and receiver is designed using VHDL after that results are verified then COFDM modulator is compared with previous work which shows the present work provides

better performance than previous work and present work utilize less number of devices than previous work. This work can be organized as: In section 2 COFDM system is explained, section 3 describes the significance of FEC with Interleaving, design details or implementation details is covered in section 4, then simulation results are described in section 5. Section 6 includes conclusion of this work and in section 7 contains the references.

2. COFDM SYSTEM MODEL
OFDM is a wireless technology patented in 1970 that turns on principle of transmitting data by dividing the data stream into multiple parallel bit stream. OFDM transmits the data by using a large number of narrow bandwidth carriers. These carriers are regularly spaced in frequency. The carriers are sent in such a way that the carriers are orthogonal, meaning that they do not cause interference to each other. Currently there are two principle 4G development technologies contending for attention: CDMA (Code Division Multiplexing) and OFDM. CDMA is well known standard and has been used for several years, but OFDM is relatively new technology which is being used by Nokia, Cisco, Lucent and Philips Semiconductor etc.

OFDM with particular channel coding scheme or with error control coding called COFDM provides the higher data rate environment with removing the effect of frequency fading and reliable data rate transmission. Thus COFDM is adopted by many wireless standards like DAB, DSL, WLAN, IEEE 802.11 a, IEEE 802.11 g, IEEE 802.11 n etc [12]. With increasing the data rate in wireless communication system time of each transmission becomes shorter. But delay time due to the multi-path fading remains constant, because of this ISI, ICI becomes main problems. COFDM avoids these problems by splitting the channel into sub-channels and transmitting the data using sub-channels in such a way that data are transmitted orthogonally so that 50% bandwidth is saved than conventional system as shown in Figure 1. Figure 1(a) shows the simple conventional method in which the bandwidth used to transmit the signal is more than COFDM as shown in Figure 1(b).

COFDM technique is another form of multi-carrier modulation which basic principles is transmission of data with reliable and at higher data rate by converting data bit into several parallel bit streams and each of these bit are modulated by each sub-carrier. COFDM signal can be presented as shown in Figure 2.

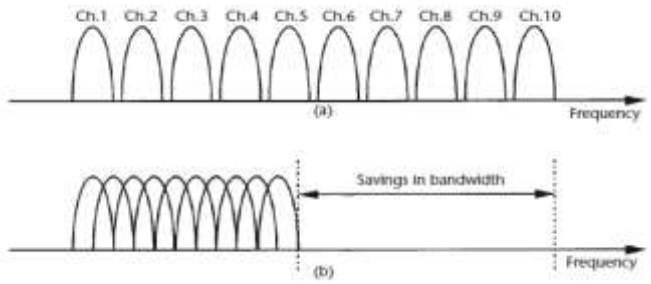
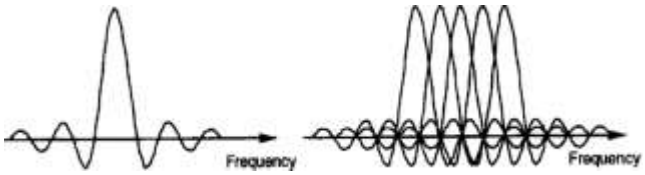


Figure 1 Transmission Techniques



(a) (b)

Figure 2 Spectra of (a) COFDM sub-channel and

(b) COFDM signal

COFDM signal generation is presented in Figure 3. To generate COFDM successfully the relationship between all the carriers must be carefully controlled to maintain the orthogonality of the carriers. For this reason, COFDM is generated by firstly choosing the spectrum required, based on the input data, and modulation scheme used. The spectrum which is desired is then converted back to its time domain signal using an IFFT. The FFT converts a cyclic time domain signal into its equivalent frequency spectrum. After performing OFDM function using IFFT & FFT, signal is send to COFDM receiver where the data transmitted through COFDM transmitter is received.

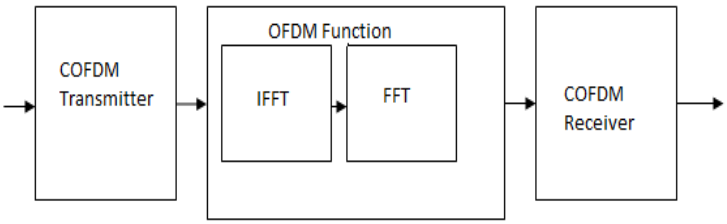


Figure 3 COFDM Generation

Basic block of COFDM transmitter and receiver is shown in Figure 4 which consists of scrambler, convolution encoder as FEC encoder, puncturer, block interleaver, QPSK scheme as constellation mapper and IFFT (Inverse Fast Fourier Transform) at transmission side. While COFDM receiver includes FFT (Fast Fourier Transform), Constellation de-mapper, de-interleaver, depuncturer, FEC decoder and descrambler. FEC encoder and FEC decoder performs FEC process at transmitter and receiver side. An IFFT and FFT block performs OFDM process to map the QPSK value into OFDM symbol so that bandwidth f Input transmission of signals is saved.

The COFDM transmitter block is divided into several parts with each block functioning differently and this is to ensure that the system works effectively. The Scrambler serializes input data Output then performs an "exclusive-OR" operation on the data [6]. Data is then encoded by the convolution encoder which is used as FEC encoder to perform FEC scheme or to encode the data and passes through puncturer. Then interleaver rearranges the bit sequence and passed through mapper after it QPSK value bit is mapped into OFDM symbols using IFFT. IFFT is performed to represent the signal or data into time domain because when data is transmitted in analog form through transmitter and represented in time domain.

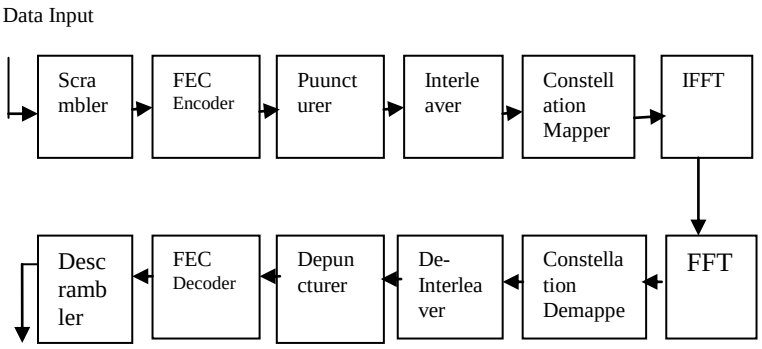


Figure 4 Basic block of COFDM Transceiver

3. FEC WITH INTERLEAVING

Interleaving is a powerful technique that is used to perform burst error correction in which the bit errors occur sequentially in time and as groups [5]. Interleaving is used in digital communications systems to enhance the random error correcting capabilities of error correcting codes to the point that they can be effective in a burst noise environment [11]. The interleaver subsystem rearranges the encoded symbols over multiple code blocks as shown in Figure 5. FEC process with interleaving enhances the performance of system with reasonable cost of price and hardware. Figure 5 shows that data is first encoded through FEC encoder then data is sent to interleaver after mapped using particular modulating scheme then transmitted, at receiving side data is first de-mapped using same modulating scheme that employed at transmitter side then sent to de-interleaver which performs reverse operation of interleaver and rearranges the data then data is decoded using FEC decoder [10].

Interleaving techniques are traditionally used to enhance the quality of digital transmission over the bursty radio channel. This is usually accomplished by scrambling successive symbols of the transmitted sequence into different time slots. A channel is considered fully interleaved when consecutive symbols of the received sequence appear to be independent not affect by the same burst error.

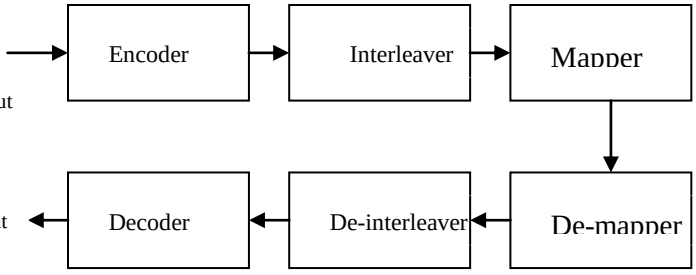


Figure 5 FEC with Interleaving

FEC coding gives the best performance when it is used with interleaving with respect to the BER (Bit Error Rate), frequency diversity, fading environment, multi-path environment etc [2]. Due to the bursty nature of many radio interference sources and the characteristics of the demodulator, it is more likely that

erroneous bits will clump together. To combat this problem interleaving of the coded data is performed after encoding in the transmitter and de-interleaving before decoding in the receiver. The main objective of interleaving is to ensure that adjacent symbols in the coded sequence are spaced out in the transmitted sequence, so that any clumps of bit errors in the received sequence are spread out more uniformly by the de-interleaver, letting the decoder work under optimum conditions [11].

4. IMPLEMENTATION DETAILS

The basic design methodology to implement the COFDM transmitter and receiver is the divide and conquer scheme in which first COFDM transceiver is divided into two main parts: COFDM Transmitter and COFDM Receiver. After it COFDM transmitter block is further divided into sub-blocks and same in case of COFDM receiver is performed. Then sub-blocks of COFDM transmitter and receiver is designed and results are verified. After verification of each block's result blocks are merged then COFDM transmitter and COFDM receiver are assembled which called COFDM Transceiver and then result of COFDM Transceiver is verified. Whole design is designed using Xilinx Project Navigator XILINX ISE 9.1i and result is verified using ModelSim XE 5.8c simulator. The device selected for this work is Virtex-5 XC5vlx30-3ff324. Basic functioning and main designing issues of each block is discussed in next.

First block of COFDM transmitter is scrambler which serializes the input data bits and used to generate the random number of sequence and work as pseudo noise sequence (PN) generator. The PN generator has applications in communications in CDMA, system testing etc [6]. In this work M-length sequence generator is used for PAPR reduction and easiest way to generate bits. De-scrambler is used to perform just reverse operation of scrambler at receiver side. Then data is encoded using convolution encoder which is used as FEC encoder to perform FEC process as shown in Figure 6. In this work convolution encoder of code rate ½ and constraint length L=3 is used to encode the data stream generated by scrambler. Viterbi decoder is used as FEC decoder at receiver side to decode bit streams. This decoder is based on "viterbi algorithm" in which the possible received bit sequence form a "tree" structure and the viterbi tracks likely paths through the tree structure [7] [8].

After this data is punctured and rearranged using interleaver, in this work block interleaver is used to remove burst type errors and bit type errors. An Interleaver spreads the scrambled data in some deterministic manner. Interleaving is a process of rearranging the data symbols so that burst error can be overcome and corrected by means of FEC which is most effective technique for it. At receiving side reverse operation is performed using depuncturer and de-interleaver to recover the data.

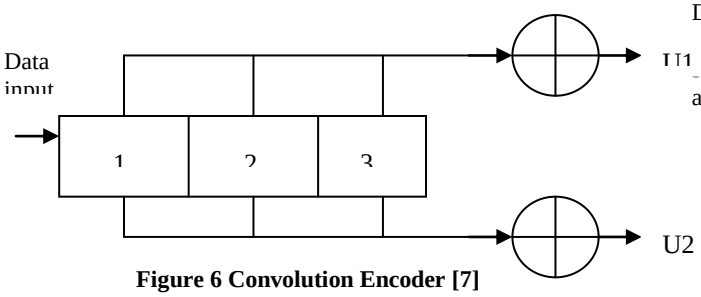


Figure 6 Convolution Encoder [7]

Then comes to the constellation mapper which is used to mapped the interleaved bits into QPSK value. The mapper converts the input data into complexed valued constellation points, according to a given constellation. Some typical constellations for wireless applications are BPSK, QPSK and QAM [14], in this work QPSK mapper is used at transmitter side. At receiver side QPSK demapper is used as QPSK mapper is used at transmitter side. The constellation graph of QPSK can be shown in Figure 7 and carrier phase shift corresponding to various input bits can be shown in Table 1.

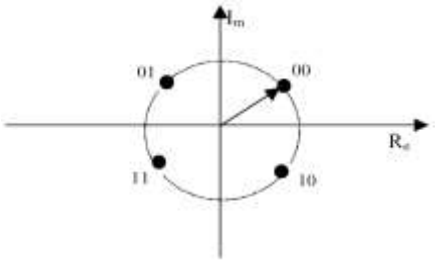


Figure 7 QPSK constellation graph [14]

Table 1. Carrier Phase Shifts corresponding to various input bits

Information bits	Phase change
11	∏/4
01	3∏/4
00	-3∏/4
10	-∏/4

To design FFT/IFFT DIT (Decimation in Time) radix-2 approach is used. FFT transforms the signals in time domain to frequency domain. In 1973 it was discovered that FFT could be used in multi carrier systems like OFDM. The equation can be written as follows

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \quad (1)$$

The quantity W_N^{nk} is defined as below

$$W_N^{nk} = e^{\frac{-j2\pi nk}{N}} \quad (2)$$

This factor also called twiddle factor is calculated and put in a table in order to make the computation easier and can run simultaneously. The twiddle factor table is depending on the number of points used, here 8-point DIT radix-2 approach is used. During the computation of IFFT, the factor does not need to be calculated since it can refer to the twiddle factor table thus it save time since calculation is done concurrently. IFFT is defined as the equation given below

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k)\, W^{-nk} \quad (3)$$

A lot of devices are utilized by IFFT/FFT block than any other block. So design the FFT/IFFT block with minimum device utilization summary is main challenge.

5. SIMULATION RESULTS

COFDM Transceiver system is designed using VHDL and synthesized using Xilinx Projector navigator XILINX ISE 9.1i. Results are verified using ModelSim XE 5.8c simulator. The design is mapped on Virtex-5 XC5vlx30-3ff324. Internal RTL view of COFDM Transmitter, COFDM Receiver and COFDM Transceiver can be shown in Figure 8, Figure 9 and Figure 10 respectively.

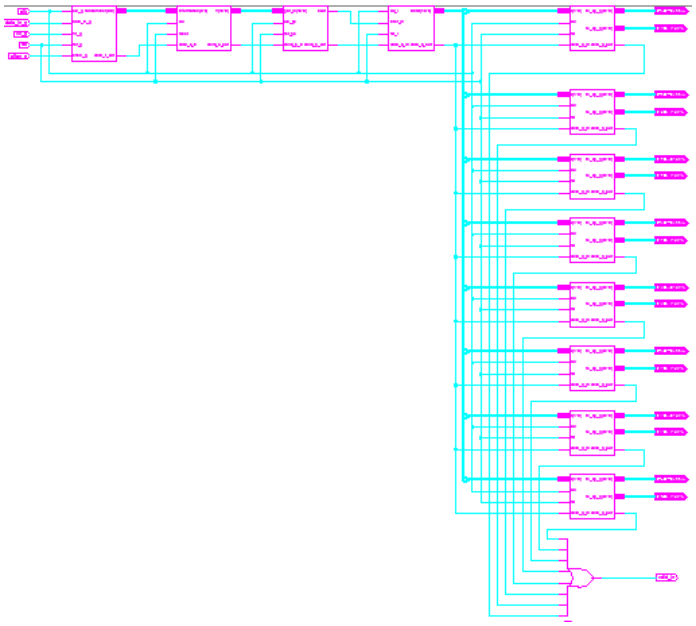


Figure 8 Internal RTL View of COFDM Transmitter

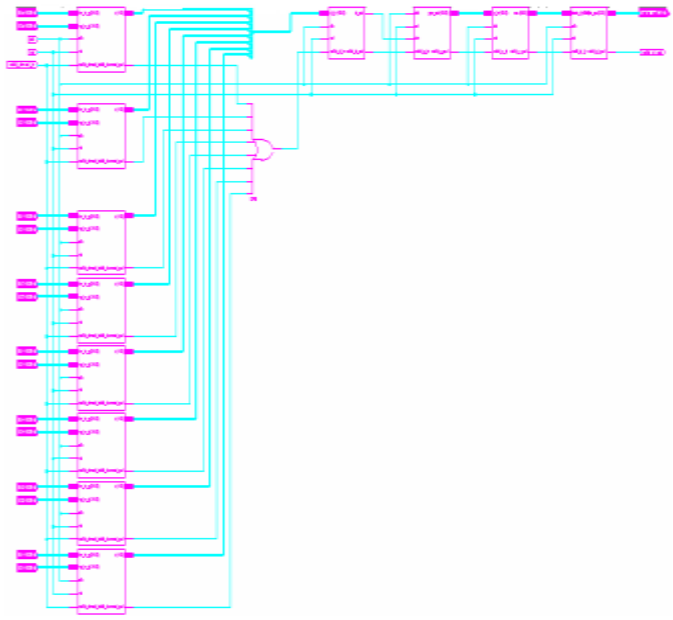


Figure 9 Internal RTL View of COFDM Receiver

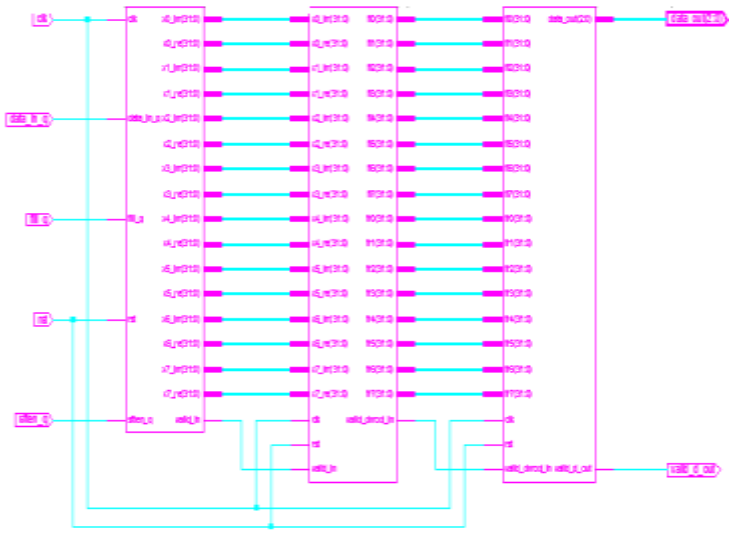


Figure 10 Internal RTL View of COFDM Transceiver

Figure 8 and Figure 9 shows the internal RTL view of COFDM transmitter and receiver which shows the combination of all blocks which are transmitter or receiver side respectively. In Figure 10 internal view of COFDM transceiver is shown which shows the combination of COFDM transmitter, COFDM receiver and OFDM blocks. Simulation results of COFDM transceiver is shown in Figure 11.

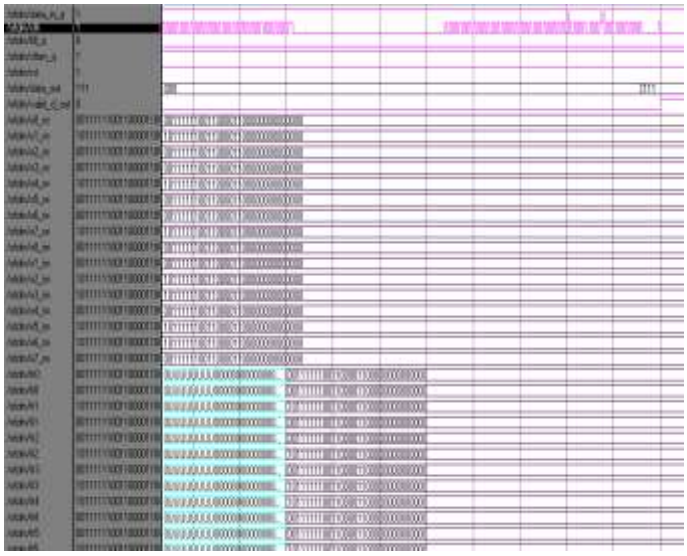


Figure 11 Simulation result of COFDM Transceiver

Simulation results verified that the transceiver would perform with suitably low bit error for the full range of coding and modulation schemes and for variation of all the channel impairments. VHDL functional verification confirmed that the HDL design exhibited good performance.

6. CONCLUSION

The main focus of this work is to shows the capability of designing and simulating COFDM system which includes OFDM integrated with FEC technique. This work's main emphasis was on designing and simulation of synthesizable VHDL code of the COFDM transceiver using Xilinx's ISE 9.1i and simulated using ModelSim XE 5.8c simulator. Device Utilization summary of COFDM Transceiver is given in Table 2. Table 3 shows the total memory used by COFDM transceiver system. Resource Utilization of COFDM modulator is compared with previous work in Table 4 and results shows the present design utilizes the less number of devices.

Table 2. Device Utilization Summary of COFDM Transceiver

Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	9263	19200	48%
Number of fully used Bit Slices	8191	61795	13%
Number of bonded IOBs	9	220	4
Number of BUFG/BUFGCTLRs	17	32	53%
Number of DSP48Es	24	32	75%

Table 3 Total Memory Used by COFDM Transceiver

Total Memory Used	196572 Kb

Table 4 Comparison of Device Utilization Summary with previous work

Logic Utilization	Present Work	Previous Work [9]
No. of Slices	754	1678
No. of slices Flip Flop	1241	2353
No. of 4 i/p LUTs	782	2814
Bonded IOB	518	29
No. of GCLKS	1	1

COFDM Modulator is compare with previous work which shows the present work utilize the less number of devices than previous work. COFDM modulator design is targeted on Vertex 2. Area, power, cost is the main constraints to design any system. This work's results shows that the presnt design utilizes less number of devices to perform better than previous work. The timing analysis of COFDM Transceiver is presented as below

Minimum period: 2.451ns (Maximum Frequency: 407.914MHz)

Minimum input arrival time before clock: 2.056ns

Maximum output required time after clock: 2.505ns

Maximum combinational path delay: No path found

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