Unipolar PWM using Trapezoidal Amalgamated Rectangular Reference Function for Improved Performance of Multilevel Inverter

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ABSTRACT
In many research papers, Pulse Width Modulation (PWM) techniques have been carried out in different angles but this paper reveals a new idea to enhance the performance of MultiLevel Inverter (MLI). An attempt is made to improve the performance of MLI and also to reduce the significant third harmonic energy by using amalgamation technique. A Trapezoidal Amalgamated Rectangular (TAR) reference signal is developed to study the performance of chosen five level cascaded MLI. To validate the developed technique, simulation and experimentation are carried out through MATLAB/SIMULINK and dSPACE respectively. Three different modulation strategies, Unipolar Amalgamated Phase Disposition (UAPD), Unipolar Amalgamated Phase Shift (UAPS) and Unipolar Amalgamated Carrier Overlapping (UACO) PWM methods are developed and implemented. Harmonic analyses are done for above amalgamated reference techniques which provide better results**.** The simulation and experimental results closely match with each other validating the strategies presented.

Keywords
MLI, PWM, Total Harmonic Distortion, UAPD, UAPS, UACO, dSPACE.

1. INTRODUCTION

A multilevel converter (DC-AC) is an emerging area in power electronic system that synthesizes a desired output voltage from several levels of DC voltages as inputs. With an increasing number of DC voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. Compared with the traditional two level voltage converter, the primary advantage of multilevel converters is their smaller output voltage step, which results in high power quality, lower harmonic components, better electromagnetic compatibility and lower switching losses. The principal motivation for multilevel topologies is the increase of power, the reduction of voltage stress on the switches and the generation of high quality output voltages and sinusoidal currents. Several multilevel topologies, namely the diode clamped MLI, the flying capacitors MLI and cascaded MLI have evolved and are applied in adjustable speed drives, electric utilities and renewable energy systems. Among the multilevel inverter topologies, cascaded multilevel inverter has more advantages than the other two. Cascaded MLIs use more than one DC voltage source to generate an AC output voltage that resembles a sine wave. Shanthi and Natarajan made a detailed comparative study of various unipolar multicarrier PWM strategies for single phase cascaded MLI through simulation using MATLAB/SIMULINK and dSPACE/RTI based implementation [1]. They also simulated and implemented carrier overlapping bipolar PWM methods for chosen single phase cascaded five level inverter in [2]. A new PWM scheme that used multiple trapezoidal modulating signals with a single triangular carrier is discussed in [3]. Multilevel PWM methods based on control degrees of freedom combination and their theoretical analysis are also discussed in [4]. A modified carrier approach that closely approximates the performance of harmonic elimination is introduced by Krein et al [5]. A modulation based method for generating pulse waveforms with selective harmonic elimination is proposed in [6]. A five level selective harmonic elimination PWM strategy based on an equal number of switching transitions compared against the previously mentioned muticarrier technique is proposed by Agelidis et al [7]. A generalized formulation for selective harmonic elimination pulse width modulation control suitable for high voltage high power cascaded multilevel voltage source converters with both equal and nonequal DC sources used in constant frequency utility applications is found in [8]. The most relevant control and modulation methods developed for this family of converters like multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination and space-vector modulation are presented in [9]. A method is presented showing that a cascaded multilevel inverter can be implemented using only a single DC power source and capacitors in [10]. A new approach to medium voltage variable frequency static AC motor drives offers improvements in power quality as in [11].This paper investigates on improved performance of PWM strategy for controlling the harmonics of output voltage of chosen MLI employing TAR reference function. Carrier disposition, phase shift and carrier overlapping PWM methods are carried out using TAR reference. The following three strategies are developed and implemented using triangular carrier and TAR reference signal: (i) Uniploar Amalgamated Phase Disposition PWM (UAPDPWM) strategy (ii) Uniploar Amalgamated Phase Shift PWM (UAPSPWM) strategy and (iii) Uniploar Amalgamated Carrier Overlapping PWM (UACOPWM) strategy.

2. MULTILEVEL INVERTER

MLIs have become an effective and practical solution for increasing power and reducing harmonics of AC load. Figure 1 shows a configuration of the single phase five level cascaded type Modular Structured Multilevel Inverter (MSMI). The MSMI is unique when compared to other types of multilevel inverters in the sense that it consists of several modules that require separate DC sources. As can be seen from Figure 1, each module of the MSMI has the same structure whereby it is represented by a single phase full-bridge inverter. This simple modular structure not only allows practically unlimited number of levels for the MSMI by stacking up the modules but also facilitates its packaging. Compared to other types of multilevel inverters, the MSMI requires less number of components with no extra clamping diodes or voltage balancing capacitors that only further complicate the overall inverter operation.

The operation of the MSMI can be easily understood. The load voltage is equal to the summation of the output voltage of the respective modules that are connected in series. The number of modules (M) which is equal to the number of DC sources required depends on the total number of positive, negative and zero levels (m) of the MSMI. It is usually assumed that m is odd as this would give an integer valued M. In this work, load voltage consists of five levels which include $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$ and $-2V_{DC}$ and the number of modules needed is 2. The following equation gives the relationship between M and m.

$$M=(m-1)/2$$

The gate signals for chosen five level cascaded inverter are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index m_a (0.6-1) and for various PWM strategies. Figure 2 depicts a sample SIMULINK model developed for UAPDPWM method. The following section briefly describes the carrier arrangements of the strategies used.

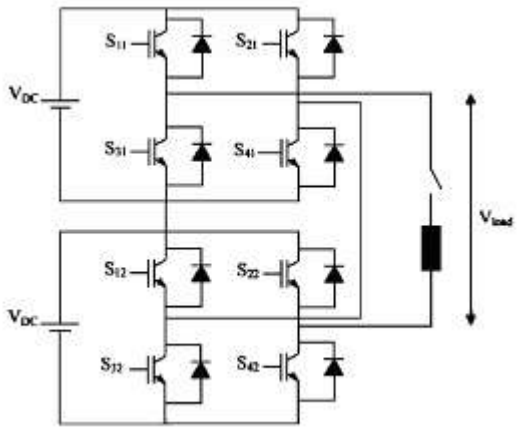

Figure 1 Five Level MSMI

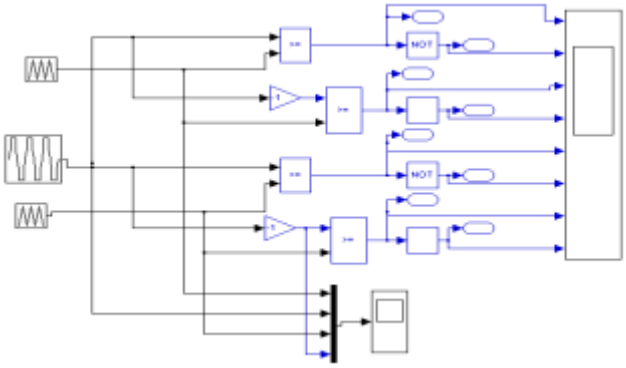

Figure 2 Sample PWM generation logic using SIMULINK model developed for UAPDPWM method

3.MODULATION STRATEGIES FOR MSMI

A number of modulation strategies are used in multilevel power conversion applications. They can generally be classified into three categories: (i) multistep, staircase or fundamental frequency switching modulation strategies (ii) space vector PWM strategies (iii) carrier based PWM strategies. Carrier based strategies are divided into two groups: single carrier and multicarrier strategies. Different multilevel topologies lend themselves to different multicarrier based PWM schemes. Multicarrier PWM methods can be categorised into two groups: Carrier disposition methods where the reference waveform is sampled through a number of carrier waveforms displaced by contiguous increments of the waveform amplitude and phase shift PWM methods where multiple carriers are shifted accordingly. Carrier based PWM methods have more than one carrier that can be triangular waves or saw tooth waves and so on. As far as the particular carrier signals are concerned, there are multiple Control Freedom Degree (CFD) including frequency, amplitude, phase of each carrier and offsets between carriers. The modulating/ reference wave of multilevel carrier based PWM strategies can be sinusoidal or trapezoidal. As far as the particular reference wave is concerned, there is also multiple CFD including frequency, amplitude, phase angle of the reference wave and as in three phase circuits, the injected zero sequence signal to the reference wave. Multicarrier PWM strategies can also be categorized into bipolar and unipolar types. This paper focuses on unipolar carrier with Trapezoidal Amalgamated Rectangular (TAR) reference function.

4. TAR BASED PWM STRATEGIES

4.1 UAPDPWM strategy

UAPDPWM strategy uses (m-1)/2 triangular carriers with the same frequency f_c and same peak-to-peak amplitude A_c which are disposed so that the bands they occupy are contigiuous. The carrier set is placed above the zero reference. Two modulation waveforms having amplitude A_m and frequency f_m. and it is centred about the zero level and are used to sample the triangular carriers to generate the gating pulses. The carrier arrangement for five level inverter using UAPDPWM is shown in Fig.3.

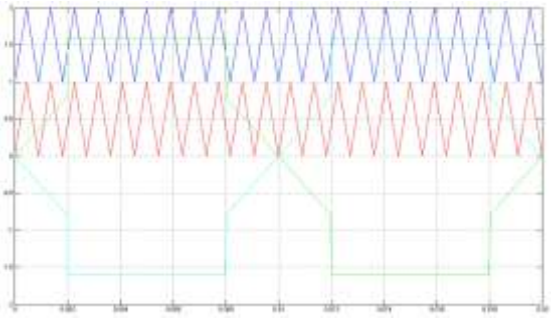

Figure 3 Multicarrier arrangement for UAPD method (m_a=0.8)

4.2 UACOPWM strategy

The UACOPWM uses two carrier signals of peak-to-peak amplitude A_c and they overlap with each other. The gate signals for this strategy are derived by comparing the two overlapping carriers with the two TAR references. Fig.4 shows the carrier arrangement for the chosen MLI with UACOPWM strategy.

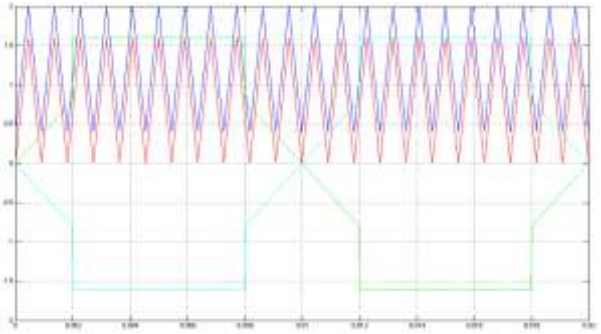

Figure 4 Multicarrier arrangement for UACO method (m_a=0.8)

4.3 UAPSPWM strategy

The UAPSPWM uses (m-1)/2 carrier signals of same peak-to-peak amplitude and frequency which are phase shifted by 360/(m-1)/2 degrees to one another to generate m level output. The gate signals for the chosen MLI are derived by comparison of two carriers with two TAR references of same amplitude and frequency but of opposite phase. Carriers for chosen five level inverter with UAPSPWM strategy are illustrated in Fig.5.

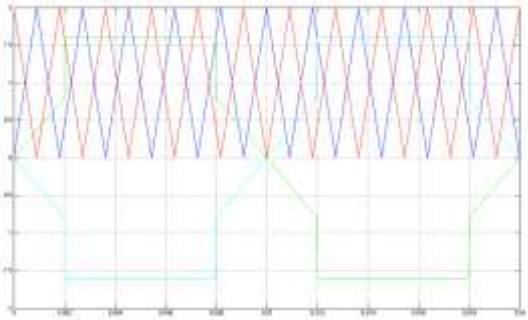

Figure 5 Multicarrier arrangement for UAPS method (m_a=0.8)

5. SIMULATION RESULTS

The cascaded five level inverter is modelled in SIMULINK using Power System block set. Switching signals for MSMI are developed using unipolar PWM techniques discussed previously. Simulations are performed for different values of m_a ranging from 0.6 – 1. Figs. 6, 8 and 10 show the simulated output voltages with chosen PWM strategies and corresponding FFT are seen plots in Figs. 7, 9 and 11 with above strategies but for only one sample value of m_a = 0.8. Table 1 displays the V_{rms} of fundamental of inverter output for same modulation indices. Among the three PWM strategies UAPDPWM and UACOPWM strategies can effectively minimize the 3rd order harmonics. It is observed from Table 2 for m_a=0.8 that the harmonic energy is concentrated more on m_f+1 and m_f-1 side bands. Minimum amount of harmonics are present in all centre frequencies i.e. m_f , $2m_f$, $3m_f$ and $4m_f$. From the Table 2 it is also visualized that in UAPSPWM strategy upper side (m_f+1) band harmonic amplitudes are relatively less than that of lower side band (m_f-1) harmonic amplitudes. It is also noticed for UAPSPWM strategy, m_f ±1, $2m_f$ ±1, $3m_f$ ±1 and $4m_f$ ±1 side band harmonics are dominant and similar dominancy exists for UAPDPWM also. The following parameter values are used for simulation: V_{DC}=100V and R (load) = 100 ohms.

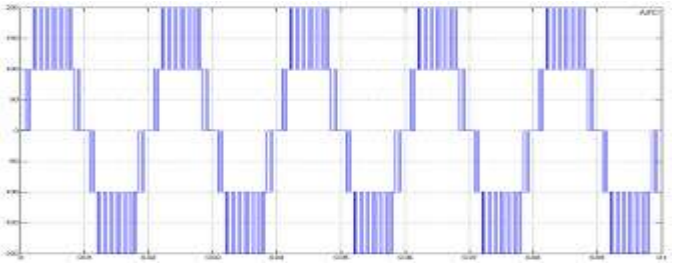

Figure 6 Output voltage generated by UAPD method

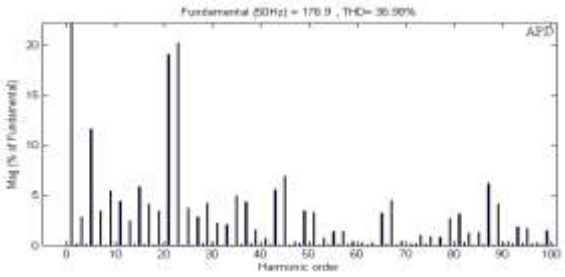

Figure 7 FFT plot for output voltage by UAPD method

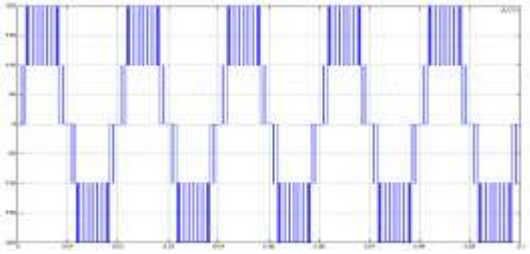

Figure 8 Output voltage generated by UACO method

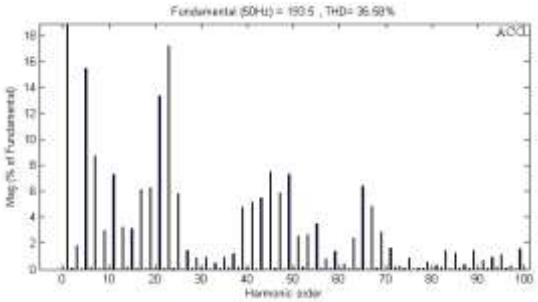

Figure 9 FFT plot for output voltage by UACO method

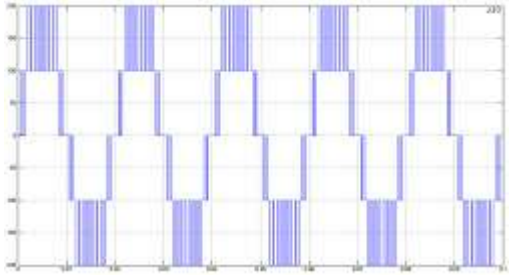

Figure 10 Output voltage generated by UAPS method

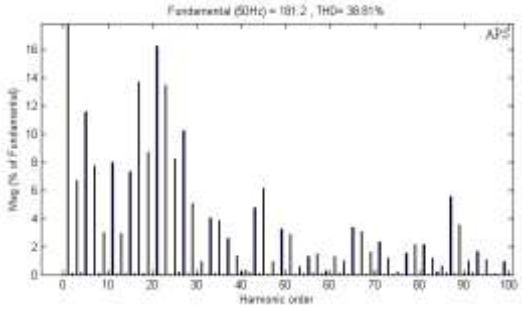

Figure 11 Output voltage generated by UAPS method

Table 1. RMS output voltage (fundamental) of different strategies (By simulation)

m_a	RMS output voltage (fundamental) with TAR reference		
	UAPD	**UACO**	**UAPS**
1	125.1	136.8	128.1
0.9	140.9	147.4	142.3
0.8	125.1	136.8	128.1
0.7	108.7	116.6	112.1
0.6	94.5	96	96.1

Table 2.Harmonic magnitude for m_a=0.8 and m_f=22 (By simulation)

Harmonic order	Harmonic amplitude with TAR reference		
	UAPD	**UAPS**	**UACO**
3 order	2.84	6.69	1.83
5 order	11.60	11.56	15.46
7 order	3.4	7.78	8.71
11 order	4.39	8.0	7.28
13 order	2.47	2.97	3.23
m_f =22	0.05	0.01	0.07
(m_f-1) 21	19.12	16.26	13.34
(m_f+1) 23	20.21	13.49	17.19
(m_f-2) 20	0.09	0.04	0.10
(m_f+2) 24	0.07	0.05	0.07
($2m_f$) 44	0	0.08	0.04
($2m_f$-1) 43	5.52	4.77	5.52
($2m_f$+1) 45	6.93	6.19	7.52
($2m_f$-2) 42	0.14	0.17	0.06
($2m_f$+2) 46	0.06	0	0.12
($3m_f$) 66	0.08	0.04	0.04
($3m_f$-1) 65	3.21	3.37	6.41
($3m_f$+1) 67	4.50	3.07	4.83
($3m_f$-2) 64	0.04	0.03	0.10
($3m_f$+2) 68	0.02	0.02	0.09
($4m_f$) 88	0.04	0.08	0.07
($4m_f$-1) 87	6.17	5.58	0.36
($4m_f$+1) 89	4.13	3.54	1.44
($4m_f$-2) 86	0.13	0.14	0.08
($4m_f$+2) 90	0.08	0.07	0.06

6. EXPERIMENTAL RESULTS

This section presents the results of experimental work carried out on chosen MSMI using dSPACE DS1104 controller board which is based on the Texas Instruments' TMS320F240 floating-point DSP. Real time implementation of these strategies using MATLAB – dSPACE/RTI requires less time for development as it can be expanded from the simulation blocks developed using MATLAB/ SIMULINK. The dSPACE system can be plugged into a PCI slot of a PC. The gate signal generation block using different PWM strategies listed above is designed and developed using SIMULINK and downloaded to dSPACE / RTI. The results of the experimental study are shown in the form of the PWM outputs of chosen MSMI. Fig.12-14 show the experimental

output voltage and corresponding FFT of the single phase cascaded seven level inverter obtained using dSPACE/RTI with various PWM strategies. Fig.15 shows the entire hardware setup. After suitably scaling down the simulation values, in view of laboratory constraints, the following parameter values are used for experimental: V_{DC}=20V and R (load) = 100 ohms.

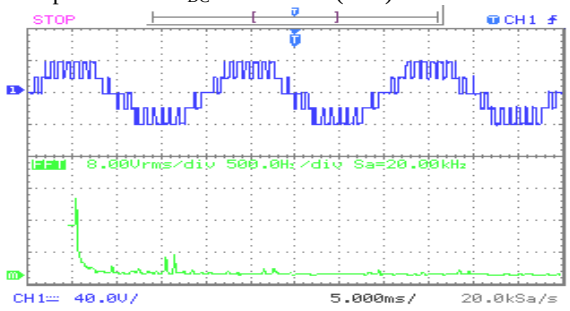

Figure 12 Output voltage and FFT of UAPD strategy

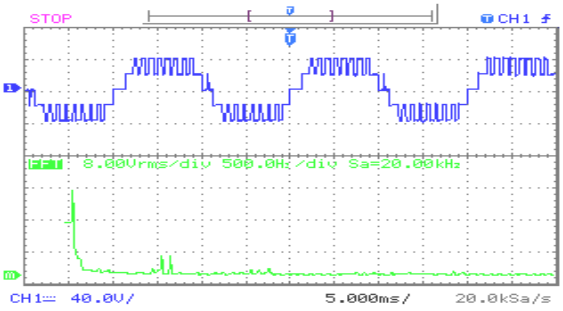

Figure 13 Output voltage and FFT of UAPS strategy

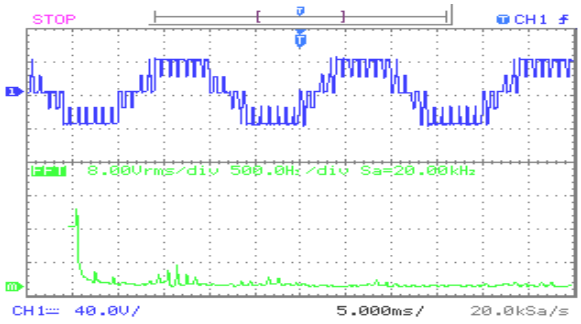

Figure 14 Output voltage and FFT of UACO strategy

Table 3. RMS output voltage (fundamental) of different strategies (By experiment)

m_a	RMS output voltage (fundamental) with TAR reference		
	UAPD	UACO	UAPS
1	22.4	23.2	22.4
0.9	20.8	21.6	19.2
0.8	19.2	20.8	17.6
0.7	18.4	19.2	16.8
0.6	16.8	18.4	16.0

Table 4. Harmonic magnitude for m_a=0.8 and m_f=22 (By experiment)

Harmonic order	Harmonic amplitude with TAR reference		
	UAPD	UAPS	UACO
3 order	1.6	0.8	0.8
5 order	1.6	0.8	3.2
7 order	0.4	0.8	0.4
11 order	0	0	0.4
13 order	0.4	0.4	0.2
m_f =22	1.6	0.8	0.4
(m_f-1) 21	4.8	5.6	4.4
(m_f+1) 23	6.4	5.2	5.6
(m_f-2) 20	0.2	0.4	1.6
(m_f+2) 24	0.2	0.2	0.2
($2m_f$) 44	0.2	0.2	0.2
($2m_f$-1) 43	1.6	1.6	1.6
($2m_f$+1) 45	1.6	1.6	1.6
($2m_f$-2) 42	0.2	0.2	0.2
($2m_f$+2) 46	0.2	0.2	0.2
($3m_f$) 66	0.8	0.4	0.4
($3m_f$-1) 65	0.2	0.8	0.8
($3m_f$+1) 67	0.8	0.8	1.6
($3m_f$-2) 64	0.2	0.2	0.2
($3m_f$+2) 68	0.2	0.2	0.2
($4m_f$) 88	0.2	0.2	0.2
($4m_f$-1) 87	0.8	0.8	0.8
($4m_f$+1) 89	0.8	0.8	0.8
($4m_f$-2) 86	0.8	0.2	0.2
($4m_f$+2) 90	0.2	0.2	0.8

Figure 15 Entire hardware setup

7. CONCLUSION

Harmonic reduction in MLIs is achieved by increasing the number of levels in the output. The process described in this paper achieves this without the need to increase the number of bridges. It is also observed from Table 2 the 3rd harmonics is minimized. Among the various PWM strategies UAPDPWM and UACOPWM strategies have minimum amount of 3rd order harmonics and UACOPWM provides maximum DC bus utilization (Tables 1 and 3).

REFERENCES

[1] B.Shanthi and S.P.Natarajan, 'Comparative study on various unipolar PWM strategies for single phase five level cascaded inverter', *International Journal of Power Electronics (IJPELEC),* Special issue on: Power Converters: Modeling, Simulation, Analysis, Topologies, Secondary issues and Applications, InderScience Pubilication, Switzerland, pp.36-50, 2009.

[2] B.Shanthi and S.P.Natarajan, 'Carrier overlapping PWM methods for single phase cascaded five level inverter', *International Journal of Science and Techniques of Automatic control & computer engineering (IJ-STA, Tunisia),* Special issue on Control of Electrical Machines, pp. 590-601, December 2008.

[3] S.M. Ayob and Z. Salam, 'A new PWM scheme for cascaded multilevel inverter using multiple trapezoidal modulation signals', *Research report of University Teknology*, Malaysia, pp.242-246, 2004.

[4] G.Carrara, S. Gardella, M. Marchesoni R. Salutari and G. Sciutto, 'A new multilevel PWM method: a theoretical analysis', *IEEE Trans.Power Electron*., vol.7, pp. 497–505, 1992.

[5] P. T. Krein, B. M. Nee and J. R. Wells, 'Harmonic elimination switching through modulation', in *Proc. IEEE Workshop Comput.Power Electron.,* 2004, pp. 123–126.

[6] R. Wells, X. Geng, P. L. Chapman, P. T. Krein and B. M. Nee, 'Modulation-based harmonic elimination', *IEEE Trans. Power Electron.*,vol. 22, no. 1, pp. 336–340, Jan. 2007.

[7] V. G. Agelidis, A. Balouktsis, I. Balouktsis and C. Cossar, 'Five-level selective harmonic elimination PWM strategies and Multicarrier phase shifted sinusoidal PWM: A comparison', in *Proc. IEEE Power Electron.Specialists Conf.*, Recife, Brazil, Jun. 2005, pp. 1685–1691.

[8] M. S. A. Dahidah and V. G. Agelidis, 'Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula', *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1620– 1630, Jul. 2008.

[9] J. Rodriguez, J. Lai and F. Peng, 'Multilevel inverters: A survey of topologies, controls and applications', *IEEE Trans. Ind. Electron.*, vol. 49, no. 4,pp. 724–738, Aug. 2002.

[10] Z. Du, L. M. Tolbert, J. N. Chiasson and B. Ozpineci, 'A cascaded multilevel inverter using a single dc power source', in *Proc. IEEE APEC*, 2006, pp. 426–430.

[11] P. Hammond, 'A new approach to enhance power quality for medium voltage ac drives', *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 202–208, Jan./Feb. 1997.