Standby Leakage Reduction in Nanoscale CMOS VLSI Circuits

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ABSTRACT
Most of the portable systems, such as cellular communication devices, and laptop computers operate from a limited power supply. Devices like cell phones have long idle times and operate in standby mode when not in use. Consequently, the extension of battery-based operation time is a significant design goal which can be made possible by controlling the leakage current flowing through the CMOS gate. This article reviews the off-state leakage mechanisms like weak inversion leakage, gate induced drain leakage and channel punchthrough current. Various circuit level techniques to reduce standby leakage and their design trade-off are discussed. Based on the surveyed techniques, a designer would be able to select the appropriate leakage optimization technique for a standby mode.

Categories and Subject Descriptors
B.7.1 [Integrated **Circuits]:** Types and Design Styles – VLSI (very large scale integration).

General Terms
Documentation and Theory

Keywords
Standby leakage, LECTOR, GALEOR

1. INTRODUCTION
Low-power consumption in high performance VLSI circuits is highly desirable aspect as it directly relates to battery life, reliability, packaging, and heat removal costs .With the continuous trend of technology scaling, leakage power is becoming major contributor to the total power consumption in CMOS circuits. Scaling of Vdd reduces dynamic power consumption but degrades the performance of the circuit as well. This can be partially compensated by lowering Vth but at the cost of increased leakage power. Minimizing leakage power consumption is currently an extremely challenging area of research, especially with on-chip devices doubling every two years. Leakage power dissipation arises from the leakage currents flowing through the transistor when there are no input transitions and the transistor has reached steady state. Unlike dynamic power, leakage power depends on the total number of transistors in the circuit, their types, and their operation status regardless of their switching activity. This makes it more difficult to attempt to reduce leakage power than to reduce dynamic power. Leakage current constitutes only of sub-threshold leakage, which is pattern dependent as it only occurs in 'off' transistors. Hence, this necessitates the need for robust techniques to reduce this leakage power dissipation. To this effect, several techniques have been proposed that efficiently minimize leakage power dissipation. This paper is organized as follows: leakage sources in an MOS transistor are discussed in details in section II; this is followed by a comprehensive survey of Standby mode leakage reduction techniques in section III. Finally, section IV gives some final conclusions.

2. LEAKAGE MECHANISMS IN STANDBY
Subthreshold Leakage current (I_{SUB}) is the most dominant leakage current component in standby mode amongst the different leakage current mechanisms contributing to the total leakage in CMOS circuits which are depicted in Figure 1[1].

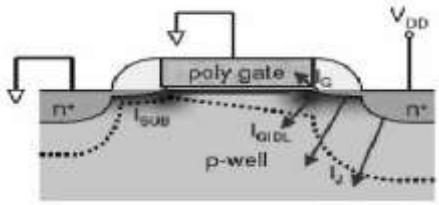

Figure 1. Different Leakage Current Mechanisms in CMOS transistor

2.1 Subthreshold Leakage:
The subthreshold current is the current between the source and the drain of the transistor in weak inversion mode, which is also known as Weak Inversion conduction Current. Subthreshold current flows by carrier diffusion rather than drift along the channel surface due to nonzero minority carrier concentration. The following parameters affect the threshold voltage and hence the subthreshold leakage current:

2.1.1 Drain-Induced Barrier Lowering (DIBL):
The barrier lowering effect is observed by a shift of threshold voltage as a function of drain voltage of short channel device. In short channel MOSFET, it is well known that the depletion

width at source and drain junction become comparable to the channel length. The effect of decreasing channel length caused the depletion region width surround the source and drain diffusion to approach each other. Depending on the drain bias, the electric field at the drain can penetrate to the source region of the device caused the decreasing of potential barrier at source. As a result, the device can conduct significant drain current due to an increase of carrier injected from the source [2]. This mechanism is responsible for the strong dependence of subthreshold current on the drain bias. Moreover the subthreshold current will change the threshold voltage as the drain bias is varied.

2.1.2 Effect of body bias

The expression (1) of threshold voltage for substrate bias reflects the influence of the nonzero source to substrate voltage upon the device characteristic as:

VT (VSB) = VTO + γ [(|2¢F|+VSB) ½ - (|2¢ F|) ½] (1)

Where, VT (VSB) is the zero substrate-bias threshold voltage which mainly depends on the manufacturing process; γ is the substrate bias coefficient (typically equals to 0.4V-0.5V) and it depends on the gate oxide capacitance, silicon permittivity, doping level, and other parameters; ¢*F* is the Fermi potential; *VSB* is the substrate bias potential. Increase in substrate reverse bias increases the threshold voltage. As per the decrease in supply voltage and body bias, leakage power decreases with decrease in threshold voltage for 45 nm technology. Hence optimal body bias is to be determined to minimize leakage.

2.1.3 Effect of temperature

Temperature dependence of threshold voltage affects the subthreshold leakage current. Increase in leakage current with temperature for a given technology [3]. Threshold voltage has temperature sensitivity of 8mV/ ºC.

2.2 Gate Induced Drain Leakage (IGIDL):

The carriers responsible for GIDL, an off-state drain leakage, originate in the region of the drain that is overlapped by the gate, under accumulation condition when the gate is grounded and the drain is at VDD. Since the substrate is at a lower potential for minority carriers, the minority carriers that have been accumulated or formed at the drain depletion region underneath the gate are swept laterally to the substrate, completing a path for the GIDL. GIDL is minimized by incorporating very high and abrupt drain doping, as it provides lower series resistance required for high transistor drive currents.

2.3 Punch Through:

Merging of the depletion regions at the drain-substrate and source-substrate junctions due to short channel and increased reverse bias across junctions is called as punch through. Subthreshold current increases due to the increase in majority carriers generated in the source and collected at the drain end due to the increase in the drain voltage beyond required punch through level. An additional implants at bottom or edges of the source and drain junction boundaries can control the punch through.

3. SURVEY OF STANDBY MODE LEKAGE REDUCTION TECHNIQUES

3.1 Self- Reverse Bias/Natural Transistor Stacks

Self- reverse biasing is a technique which helps to reduce subthreshold leakage current by turning off a stack of transistors [4]. This *stacking effect* is achieved by exploiting the dependency of subthreshold current on source voltage VS as depicted in figure 3. Increase in VS results in:

- Negative VGS if the applied input is grounded,
- Decreases signal strength (VCC-VS),
- Reduces DIBL due to reduction in VDS causing leakage reduction
- Negative VBS (body effect);

thereby reducing sub threshold leakage current exponentially. More are the number of off transistors in a natural stack; less is the leakage due to raised source voltage as shown in figure 4. Sub threshold leakage through logic gate is dependent on applied

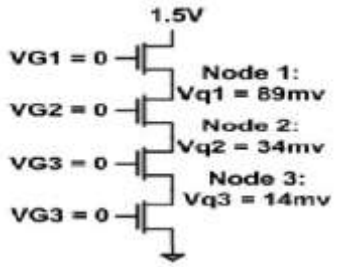

Figure 2. Leakage current descendants with the number of transistors OFF in stack

input vector. But under high gate leakage conditions, natural stacking fails to reduce leakage; rather it might increase the overall leakage [5]. However, circuits in which natural stacking does not exist; forced stacking is used [6]. Forced stacking utilizes the stacking effect by introducing an additional transistor for every input of the gate in both NMOS and PMOS networks. By replacing a single transistor of width W by two transistors each whose width is W/2 ensures that two transistors are OFF instead of one for every OFF-input of the gate which makes a significant savings on the leakage current. Reducing leakage through the use of transistor stacks depends on the choice of input pattern during standby periods since it determines the number of OFF transistors in the stack.

The work in [7] exploits an idea of an effective stacking of transistors in the path from supply voltage to ground. Two leakage control transistors (LCTs) are introduced in each CMOS gate such that one of the LCTs is near its cutoff region of operation. Drawbacks like propagation delay and area overhead

are overcome by transistor sizing and using SCCG gates for LECTOR (LEakage Control TransistOR) respectively.

In [8], a technique called as GALEOR (GAted LEakage TransistOR) is introduced which achieves 52% savings in leakage power compared to 30% power reduction obtained using LECTOR which is depicted in figure 4. Area overhead is minimized by eliminating the use of control logic to switch between the active and standby states.

3.2 Sleep Transistor, MTCMOS and Power Switches

Another way for leakage current control is inserts sleep transistor in series with the pull-down/pull-up path of a gate.There are two insertion schemes-PMOS and NMOS insertion. Due to the advantages like smaller resistance at the same width and smaller size, NMOS scheme is preferable than PMOS scheme [9].

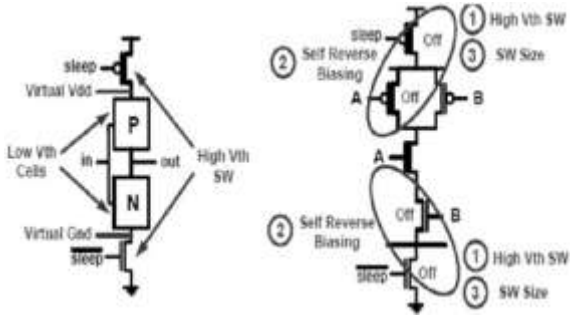

Figure 4. Power Gating Circuit and Mechanisms

In such a circuit, the supply voltage is turned off during the standby mode by using a PMOS transistor or an NMOS transistor. In active mode, the sleep transistor is on and the circuit functions as usual. The basic mechanism by which the switch transistor reduces the leakage current of the power gated logic transistors is the increased body effect: the increased source voltage of the logic transistors, relative to their bodies, raises their thresholds [10]. The resulting current flow from the power or to the ground is substantially reduced. Since this high V_{th} sleep transistor acts as a current gate to the designed circuit, this technique is also referred to as Power Gating. Power gating circuit and leakage reduction mechanisms are depicted in Figure 4 [11]. The topology, which is known as MTCMOS described in [12] and [13], reduces leakage effectively by inserting a high-threshold voltage sleep transistor in series with the power supply and the existing design and ground. MTCMOS can only reduce leakage power in standby mode and the large inserted sleep transistors can increase the area and delay. Sizing of the sleep transistors is an important design consideration. Usage of large transistor solves the delay problem incurred due to voltage drop; but it increases the area overhead and the dynamic power consumption. To reduce this area and power overhead, one transistor can be used for each group of gates rather than each logic gate. The Power switch transistors which are inserted in-between the logical circuit and the supply/ground lines are very effective in cutting the leakage currents in a standby mode by de-supplying unused blocks. MTCMOS technique, as discussed earlier, can significantly reduce the subthreshold leakage currents during the circuit sleep (standby) mode by adding high-V_{th} power switches (sleep transistors) to low-V_{th} logic cell blocks. As supply voltage is scaling down continuously, high V_{th} transistors cannot operate with supply voltages equal to or below than 0.7V. To cope with this issue, the Boosted Gate MOS scheme [14] was introduced. The gate overdrive of this high- V_{th}, thick gate oxide transistor is drastically improved by applying a higher than gate-to-source voltage. This scheme has the added advantage of lowering the gate tunneling currents. The MVCMOS [15] is similar to Super Cutoff CMOS power switch [16]. It is a low- Vth transistor whose leakage current is exponentially reduced by reverse-biasing its gate, rendering the gate-to-source voltage negative in the case of an nMOS transistor and positive in the case of a pMOS one. The main advantages of this power switch are its small size and the fact that it performs pretty well in a low- V_{th} environment. To achieve maximum leakage reduction, automatic gate biasing of Super Cut-off CMOS (SCCMOS) switch [17] is done using a polarization circuit that automatically finds the optimal gate bias voltage whatever the environment condition.

3.3 Body Biasing

Power consumption can be reduced by using low supply voltage and low threshold voltage without loosing speed performance; but it leads to increased subthreshold leakage and hence standby power consumption. One of the methods proposed to solve this problem is VTCMOS which utilizes body effect. The threshold voltage of the low threshold devices is controlled by applying variable substrate bias voltage V_{bs}. This is varied by making the substrate voltage lower than ground for NMOS transistors and higher than supply voltage for PMOS transistors. The advantage of VTCMOS scheme is no extra circuit is required for the data retention. But VTCMOS needs triple well technology to achieve different substrate bias voltage levels which adds complexity of structure as shown in figure 11. It also needs separate substrate bias voltage generator.

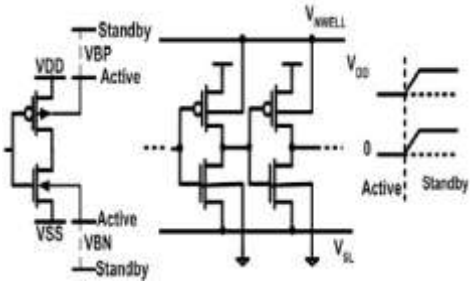

Figure 5. VTCMOS Scheme

Body biasing techniques use the body terminal bias values as another control mechanism to dynamically tune threshold voltages. Reverse body biasing is often used to reduce the device leakage power. For every process technology there is an optimum reverse body bias. Article [18] proposes a new optimal body biasing system to balance the subthreshold leakage with the BTBT leakage. In this, the threshold voltage is increased by adjusting body-bias voltage in RBB direction and when the optimal body bias is reached, the body voltage adjustment is stopped to avoid excessive reverse body bias.

4. CONCLUSION

As technology scales down to the deep sub-micron (DSM) domain, chip power dissipation and power density are increasing rapidly. With deep-submicron and nanometer technologies, the leakage current becomes more critical in portable systems where battery life is of prime concern. In view to this, we stress the importance of leakage current in CMOS circuits. In this paper, several leakage mitigation techniques are explored that can control standby leakage. Based on the surveyed techniques, a designer would be able to select the appropriate leakage optimization technique for a particular level of an application.

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