Zero-Voltage and Zero-Current Switching Converters

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ABSTRACT

This paper deals with the simulation of a PWM three-level (3L) & five level (5L) converters. The modulation strategies can be classified into two kinds according to the turn-off sequence of the two switches of the pair of switches. The concept of the leading switches and the lagging switches is introduced to realize soft-switching for PWM 3L and 5L converters. soft-switching obtained by using both the leading switches and the lagging switches. soft-switching PWM 3L and 5L converters can be classified into two kinds: zero-voltage-switching (ZVS) and zero-voltage and zero-current-switching (ZVZCS), A three level & five level ZVZCS converters are presented, its operation principle, and the simulation results obtained by using PSPICE are included also.

Keywords-ZVS,ZCS, PWM,

I. INTRODUCTION

POWER factor correction (PFC) techniques are widely used in power conversion applications to comply with IEC61000-3-2 standard. For three-phase PFC converters, the output voltage is 800 V, and may be even higher than 1000 V to reduce the input current harmonics, which raises the voltage rating of the switches of the downstream dc/dc converter, for which it is very difficult to select suitable power switches. In order to overcome this problem, Pinheiro and Barbi proposed the concept of three-level (TL) converter, in which the voltage stress of the power switches is only the half of the input dc voltage [1]. In recent years, there are several soft-switching PWM TL converters presented [1]–[3]. The objects of this paper are to reveal the relationship among Three level and five level topologies and modulation strategies,and choose suitable modulation strategies for soft-switching PWM 3L and 5L converters. Based on the analysis of the operation principle of TL converter Section II description of 3L and 5L converters. Section III classifies the modulation strategies into two kinds according to the turn-off sequence of a pair of switches. The concept of the leading switches and the lagging switches is introduced to realize soft-switching. Section IV simulation results analyzes the realization of soft-switching for both the leading switches and the lagging switches.

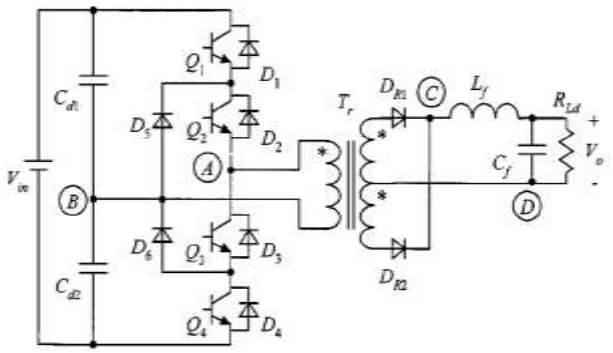


Fig. 1 Three level converter

II. DESCRIPTION OF THRE & FIVE LEVEL CONEVRTER

A. 3 level converter

Fig. 1(a) shows the basic 3Lconverter, where the capacitors Cd1 and Cd2 are large enough and equal to share the input voltage Vin evenly, i.e., .Vd1 and Vd2are clamping diodes. By modulating the four switches, Q1 tp Q4, the voltage between point A and B ,VAB , is an ac square voltages which amplitude

is Vin/ 2. is transferred by the transformer Tr and rectified by the output rectifier diodes DR1and DR2 , and then VCD is a dc square voltage pulse, which amplitude is Vin /2k , where k is the primary and secondary winding ratio. By filtering VCD, we can get the dc voltage , the output voltage. In order to get VCD ,we just need to make VAB be an ac square voltage which amplitude is Vin/2 . The fundamental modulation strategy is shown in Fig. 1(b). The upper pair of switches Q1 and,Q2 or lower pair of switches, Q3 and Q4 turn on/off simultaneously. The on-time Ton of each switch is determined by the duty cycle D of VCD, Ton = D.Ts/2 , where Ts is the switching period. By observing the fundamental modulation strategy, we could get a new idea shown in Fig. 1(b). Based on the fundamental modulation strategy, we can

1) keep the on-time of Q2 and Q3 unchanged, push the on-time of Q1 and Q4 forward or even make it be equal to ; or

2) keep the on-time of Q1and Q4 unchanged, push the on-time of Q2 and Q3 backward or even make it be equal to TS/2 ; or

3) push the on-time of Q1and Q4 forward or even make it be equal to TS/2, and VAB at the same time, push the on-time of Q2 and Q3 backward or even make it be equal to , is just the same as the fundamental modulation strategy, this is because that only and turn on simultaneously, is the positive voltage, (+ 1)Vin/2 , and only Q3 and Q4 turn on simultaneously, is the negative voltage, (-1)Vin/2 . So providing the overlap on-time of the upper pair of switches or the lower pair of switches unchanged, i.e., Ton(overlap) = D.TS/2, pushing the on-time of the switches forward or backward will not effect VAB .

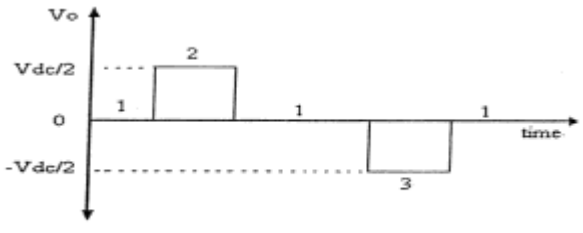


Fig. 2 stepped output voltage of 3L-ZVZCS converter

B. Five level converter

m - 1 capacitors on the dc bus and produces m levels of the phase voltage. Fig. 3 shows a fivelevel diode-clamp converter in which the dc bus consists of four capacitors, C1,C2,C3,and C4,. For a dc bus voltage Vdc, the voltage across each capacitor is Vdc/4, and each device voltage stress will be limited to one capacitor voltage level, Vdc/4, through clamping diodes. To explain how the staircase voltage is synthesized, the negative dc rail, 0, is considered as the output phase voltage reference point. Using the 5-level converter shown in Fig. 1 as an example, there are five switch combinations to synthesize five level voltages across V3 and VS.

1) For voltage level V3S =- Vd,, turn on all upper switches S1 to S4

2) For voltage level V3S = 3Vdc/4, turn on three upper Switches S2 through S4 and one lower switch S5.

3) For voltage level V3S = Vdc,/2, turn on two upper switches S3 and S4 and two lower switches S5 and S6

4) For voltage level V3S = Vdc/4, turn on one upper switches S4 and three lower switches S5 through S7

5) For voltage level V3S = 0, turn on all lower half switchesS5 to S8

Table I Switching states of 3 level converter

Output voltage van	Switching Sequence			
	S_1	**S_2**	**S_3**	**S_4**
0	**0**	**0**	**0**	**0**
Vdc/2	**1**	**1**	**0**	**0**
-Vdc/2	**0**	**0**	**1**	**1**

Table II Switch states of 5 level converter

Output Voltage V_{3S}	Switching Sequence							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0	1	1	0	0	1	1	0	0
Vdc/4	1	1	1	0	1	0	0	0
Vdc/2	1	1	1	1	0	0	0	0
^ -Vdc/4	1	0	0	0	1	1	1	0
^ -Vdc/2	0	0	0	0	1	1	1	1

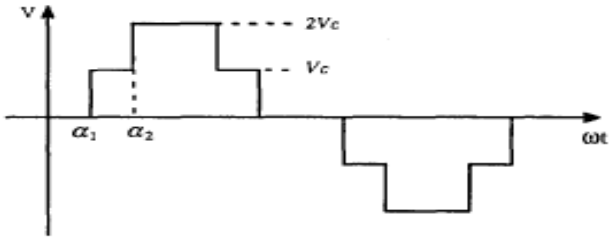


Fig. 3 stepped output voltage of 5 level inverter

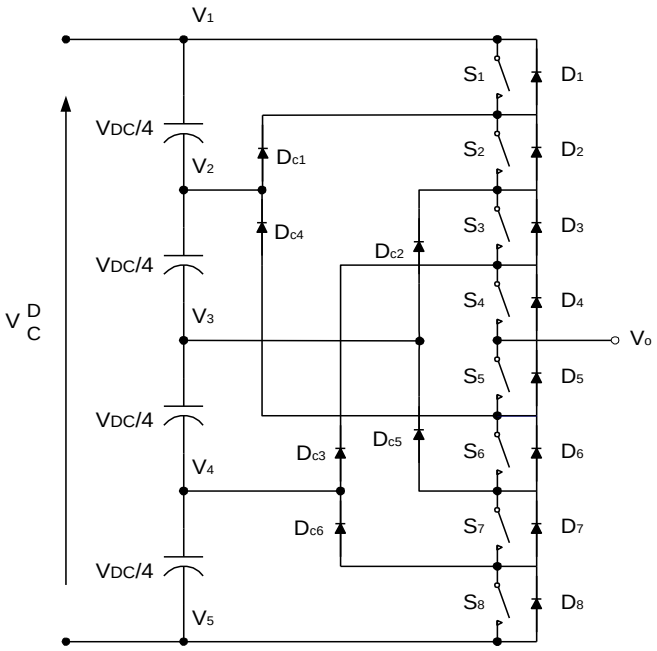


Fig.4 Five level inverter

III OPERATING MODES AND DESCRIPTION OF ZVSZCS OPERATION

C. Operating modes 3 level converterr

Mode1: During mode 1,the switching pair S1 and S3 and switching pair S2 and S4 are turned off, the voltage level of the output voltage Van=0.

Mode 2: During mode 2, switches S1 and S2 are turned on,the voltage level of the output voltage Van=Vdc/2.

Mode 3: During mode 3,switches S3 and S4 are turned on, the voltage level of the output voltage Van= -Vdc/2.

Operating modes 5 level converter

Mode 1 : During mode1 S1, S2, and S5 &S6 are turned on and remaining switches are in turn off condition,in this mode level of the output voltage V3S= 0

Mode2 During mode 2 S1,S2,S3 and S5 are turned on and remaining switches are in turn off condition, in this mode voltage level of the output voltage V3S = Vdc/4

Mode 3: During this mode S1,S2,S3,S4 are turned on and voltage level of the output voltage V3S= Vdc/2

Mode 4: During this mode S1,S5,S6 and S7 are turned on and voltage level of the output voltage V3S = -Vdc/4

Mode 5: during this mode S5,S6,S7,S8 are turned on and voltage level of the output voltage V3S = -Vdc/2

D. 3L-ZVZCS Waveforms

The main circuit of ZVS PWM 3L converter refers to Fig. 1 where Q1 and Q4 are the leading switches, Q2 and Q3 are the lagging switches. Fig. 4 shows the key waveforms for ZVZCS PWM 3L converter. The lagging switch is zero-voltage turn-off thanks to their paralleled capacitors. Similar to ZVS PWM 3L converters, the leading switches can realize zero-voltage turn-off thanks to their paralleled capacitors. Now we consider the turn-on of the leading switches. Refer to Fig.4, as Q1 zero-voltage turns off at t0 , the converter is in zero state, ip will decay to zero at t1. If Q4 do not turn on before t1, C4 will be recharged, which make lose zero-voltage turn-on condition. The time for ip to decay to zero is related with the load. In order to ensure zero-voltage turn-on for Q4 under any load, Q4 should turn on just as Q1 turns off, which means that the on-time of Q4 should be pushed forward to be TS/2. Similarly, the on-time of should also be pushed forward to be TS/2. No capacitors are in paralleled with the lagging switches to ensure ZCS. As shown in Fig. 4, ip decays to zero at t1. In order to ensure zero-current turn-off Q2 , should be delayed to turn off at t1 ,t01 = t1-t0 is related with the load. During [t1,t2], ip keeps at zero, so the turn-off time instant of Q2 can also be delayed to t2, i.e., the on-time of Q2can be pushed backward to be TS/2 ,Q3 is similar to Q2. In a word, the lagging switches have two kinds of on-time.

Similarly five level converter operates in ZVZCS mode leading switches are turned on at zero voltage and lagging switches are turned-off at zero current, main advantage of this soft switched converters are low switching stresses and current tails across switches are reduced.

PSPICE simulation diagrams :

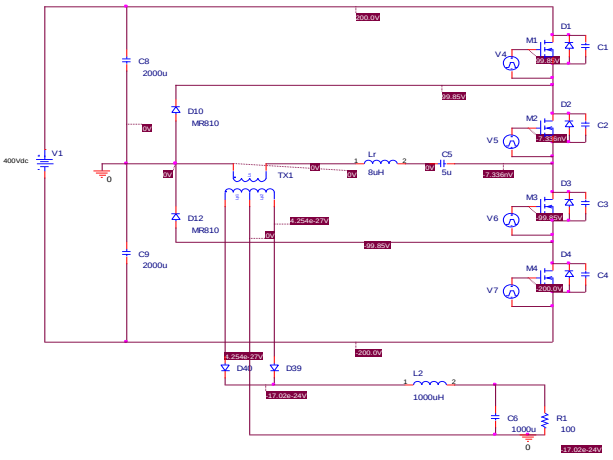


Fig: Three Level

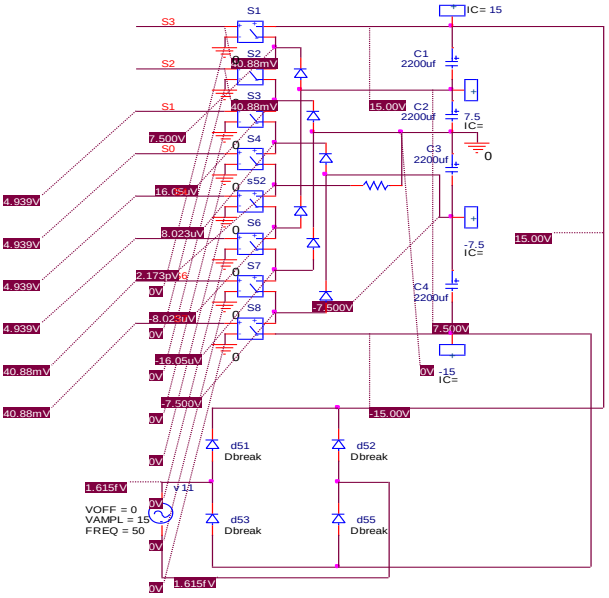


Fig: Five Level

IV SIMULATION RESULTS OF 3L-ZVZCS INVERTER AND 5L-ZVSZCS CONVERTER

A.3L-ZVZCS inverter

Simulations are conducted for 3L-ZVZCS converter by using PSPICE. Fig 5 & 6 show s that stepped output voltage and load voltage. Fig.7 & Fig. 8 shows that stepped output voltage of 5L-ZVZCS converter and voltages across S2,S3,S4,S5,S6. parameters used in simulation are shows in TableIII .

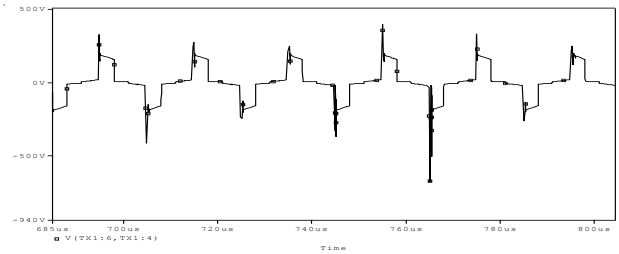
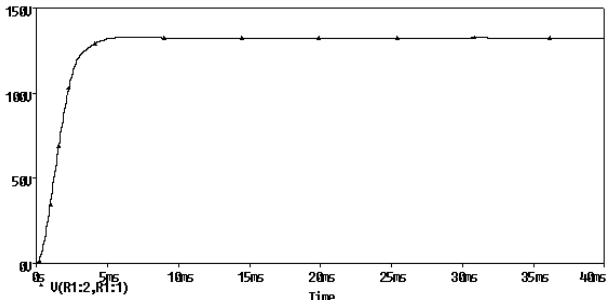


Fig. 6. Stepped output voltage of 3LZVZCS



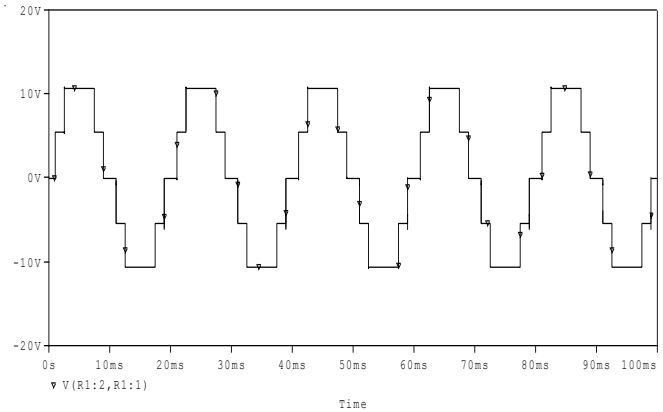
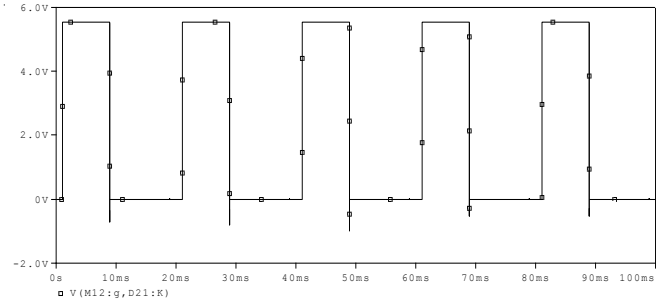
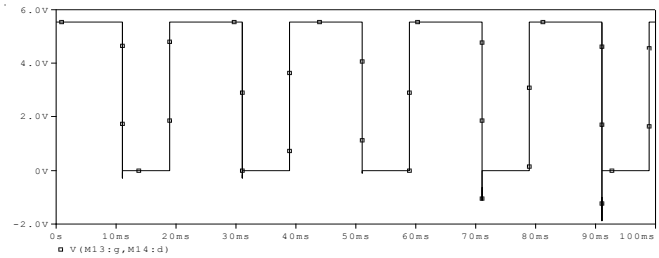
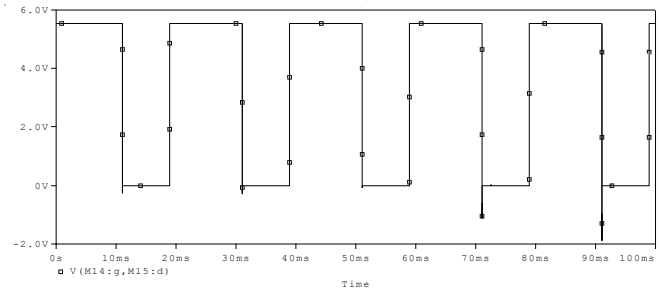
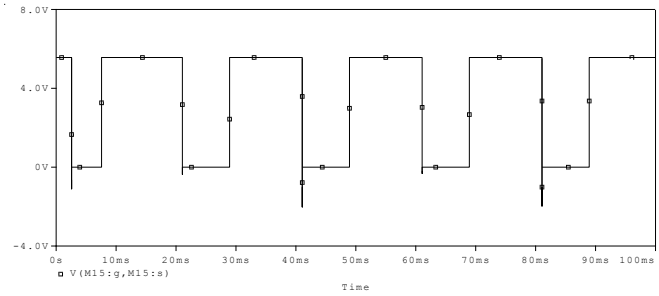


Fig 7.stepped output voltage of 5L-ZVZCS inverter









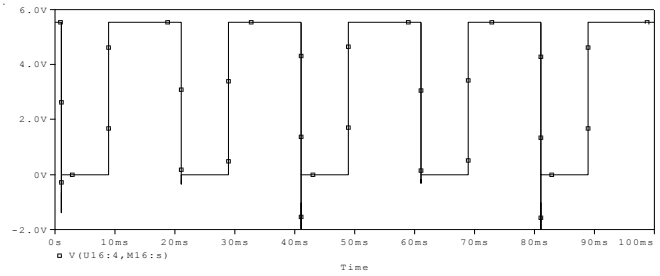


Fig. 8 Voltage across S_2,S_3,S_3,S_4,S_5 and S_6

TABLE-III SIMULATION PARAMETERS

S_1,S_2,S_3,S_4, S_5,S_6, S_7, S_8	IRF 540
Diodes	MR 810
Input voltage (3L)	400vdc
Output voltage(3L)	220vac
C1,C2,C3,C4 (5L)	2200µF
C1,C2,C3,C4 (5L)	2000µF
L2	1000 µH
Input voltage (5L)	30vdc
Output voltage	30vac

V CONCLUSION

The soft switched pwm three-level and five level converters are simulated using PSPICE software. Simulated waveforms arecoinciding with theoretical results According to the above analysis, we can draw the following conclusions.

1) Soft-switching ZVS, ZCS which introduces the concept of the leading switches and the lagging switches;

2) The leading switches are easy to realize ZVS and they can only realize ZVS;

3) Zero state has two kinds of operation modes: current constant mode and current reset mode; In constant current mode, the lagging switches can realize ZVS; and in current reset mode, the lagging switches can realize ZCS;

4) Soft-switching PWM 3L and 5L converters can be classified into two kinds: ZVS and ZVZCS and the operation principle and the simulation results are also included.

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