CMOS Development and Optimization, Scaling Issue and Replacement with High-k Material for Future Microelectronics

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ABSTRACT:

The development and optimization of Silicon technology has been guided by CMOS scaling theory [1] and predications made by Semiconductor Industry (SIA) in the International Technology Roadmap for Semiconductor (ITRS). With the trend of scaling down of Complementary Metal Oxide Semiconductor (CMOS) transistor as Moore's Law [2] requires replacement of conventional silicon dioxide layer with the higher permittivity material for gate dielectric. As the silicon industry moves to 32nm technology node and beyond complaints like leakage and power dissipation dominates. Managing such issues are crucial factors for reliable high speed operation and chip design. Although scaling will continue for couple of decades but device geometries reaches to atomic size and limitation of quantum mechanical physical boundaries. To address these problems there is need of innovation in material science & engineering, device structure, and new nano devices based on different principle of physics. Here we have elaborated about scaling issues and alternate high-k dielectric for Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Introducing a high-k material may replace today's silicon dioxide technology and can also provide extendibility over several generations. C-V analyses have been studied for various MOS capacitor with conventional SiO_2 and also with high-k material like Gd_2O_3, ZrO_2, HfO_2, and TiO_2.

Key words: Scaling, High-k, Material oxides

1. INTRODUCTION:

The fundamental building blocks for all computer chips—transistors—have tracked with Moore's Law for forty years. The transistors manufactured today are 25 times faster than and occupy less than 1% of the area of those builds four decades ago. In the past four decades the downsizing /scaling of MOSFET results to smaller device in smaller area, consumption of less power, and decrease in cost per transistor per function cost of integrated circuit.

1.1 SCALING ISSUES OF CMOS CIRCUITS:

The constraint for technology to scale insist that the total power consumption per unit area remains constant which means that as density of the circuitry in a technology increases, the amount of cooling requirement for the circuit remains constant- if this was allowed to increase after some point, the circuit would melts [1]. Many limitations for the down scaling have been proposed in the literature [1,3] Table1. Unfortunately the thickness gate silicon dioxide reaches its thinnest limit. Now further scaling oxide layer is not capable to maintain insulating property, since direct tunneling dominates the leakage current further down scaling leads several physical and technological limitations.

1.2 SCALING PREDICATIONS AND PRESENT ERA:

Most important research paper which specifies the research required to continue rapid development in semiconductor industry is International Technology Roadmap for Semiconductor (ITRS. The scaling dimensions have reduced to a factor 1000 during last 40 years (fig-1). The further reduction in gate insulator thickness leads to short channel effects, drain-voltage-induced barrier lowering, and increase to leakage current. ITRS says that the silicon technology will continue to shrink with its historical rate of predictions with Moore Law for decades [4]. Every other year new assessment is published and reduction in gate length has been observed to even faster than the predication fig-1 and table-2. In 1958, the integrated circuit was born when Jack Kilby at Texas Instrument. The research in this field saw the evolution of the (MOSFET) in 1960and the invention of Complementary Metal Oxide Semiconductor (CMOS) transistors in 1963.In 1970 because of short channel effects and the resolution of the optical lithography limit for channel was considered to be one micrometer.

Table-1 The scaling rule for device parameter by a unitless scaling factor á with possible solution for smarter, faster, lower power dissipation, and lower cost IC

Microelectronics parameter	Scaling Factor	Limiting factor	Solutions
Voltage V_{dd}	1/â	Thermal Voltage/quantum confinement	Low operating temp.
Electric Field	1		
Channel Length L	1/â	Lithography	Double Gate structure

Drain Current	1/â	Punch through	(DG FET)
Gate capacitance per unit area, $C_{ox} = \varepsilon_{ox}/D$	â	Physical thickness Limit Non Scalabilities Leakage current	Oxynitride /high-K Atomic layer deposition (ALD)
Gate area, $A_g = L * W$	$1/â^2$		
Gate capacitance $C_g = \varepsilon_o A/d$	1/â		
Parasitic capacitance C_x	1/â		
Carrier density in channel, $Q_{on} = C_o V_{gs}$ **Channel resistance $R_{on} = 1/WQ_{on}$**	1 1		High mobility material/strained devices/ Chemical process
Gate propagation delay T_{pd}	1/â	Non Scalable V_{dd}	
Maximum operating frequency, f_o	$â^2$	Parasitic capacitance, EMI, interconnect R & C	Low K-insulator Copper
Saturation current, I_{dss}	1/â	Gate leakage current Frequency of transistor Over heating	Smart system power management Physical thicker gate dielectric High – k-dielectric
Current density, J	â		
Switching energy per gate $E_g = I C_g (V_{DD})^2 / 2$	$1/â^3$		
Power dissipation per gate, P_g $P_g = P_{gs} + P_{gd}$ Both P_{gs} and P_{gd} are scaled by	$1/â^2$		
Power dissipation per unit area **$P_a = P_g/A_g$ is scaled by α^2/β^2**	1		
Power speed product, $P_T = P_g T_d$	$1/â^3$		
Transistor per chip n	$â^2$	Yielding, complexity in interconnection	Serial signal communication

A general scaling rule of MOS devices

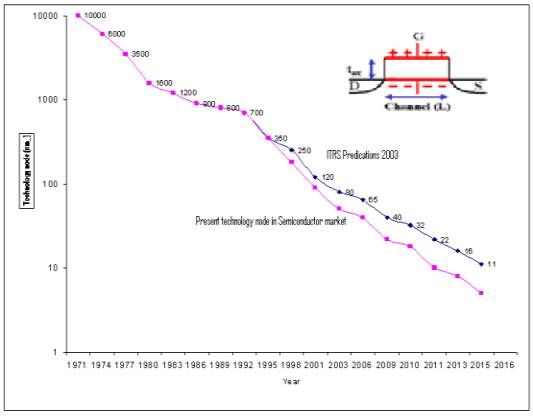


Fig-1 MOS channel length scaling and predication made by ITRS 2003 (blue line) and physical channel length (pink line)

In 1980 limitations were increased source/drain resistance, direct tunneling through gate oxide and dopant fluctuation in Short channels results to half to quarter micron [5]. While in 1990, 100 nm was thought to be limit because of some physical parameter and increase of fundamental atomistic vibrations.

1.3 CURRENT ISSUES IN SCALING OF SUB-32 NM DEVICES

The ITRS is most important industrial strategy paper for semiconductor devices & technology towards high performance and lower cost. ITRS is organized by the Semiconductor association of Europe, Japan, Korea, Taiwan and the USA. The representative from leading semiconductor

companies around the world agrees on several issues one of them was physical gate length of microprocessor [13]. Currently the "International Technology Working Groups" (ITWG) USA, is responsible for technologies and methodologies used for future area of research. The "National Technology Roadmap of semiconductor (NTRS) and ITRS have scaling predication from 100 components per IC in 1965 to 15 billion in the current state of art. There are less gain in device performance i.e power consumption, short channel effects and parasitic capacitance as scaling goes further below sub-100 nm [5,14]. In 2007 the use of high-K dielectrics is introduced for the first time, to address gate leakage issues.

The performance of MOS transistor below 30 nm in still below satisfactory and also the characteristics across wafer is also of great concern. Because of downscaling the gate length and gate oxide thickness decreased only 100, supply voltage decreased by factor 10, chip area increased by 10 and power dissipation increased by 10^5, which may not increased under ideal scaling. The major difficulties are tremendous cost of lithography and in developing new technologies [10]. In table-2 column 1 shows technology node which means the smallest poly-Si/metal gate length and column 2 shows expected starting year. It is being noted that neither 22 nm nor 16 nm numerical value appearing value in the corresponding ITRS parameter sets. The device less than 10nm gate length would be extremely sensitive to the device physical dimensions and variations in material composition. The literature clearly states that 0.1 nm oxide, a 0.1 increase in the root-mean-square (RMS) interface roughness can lead to 10 fold increase in gate leakage current [12-13]. So growth of such films must be precisely controlled on atomic scales. Also searching for ultra thin gate dielectric need to be investigated and then integrated with silicon technology. Due recent economical depression all the semiconductor companies except Intel reduced the budget for R & D. In future there is possibility on more delay in the trend of gate-length shrinkage, Equivalent gate oxide thickness and the depth of junction. In this review paper recent development and the progress of the ultra thin gate dielectric material is summarize. Presently sub-100 nm MOS transistor is in production and 6nm gate length is under research.fig-3 [6]. Recently 2009-2010 Intel corporation manufacturing transistors have set a record I_{on}/I_{off} characteristic with different metal gates and high K-dielectric material.

Table-2 Gate dielectric layer technology requirement [8-10].

Technology Node (nm)	Starting year	ITRS updates			T_{inv} (nm)	EOT(nm)
		Years	Half pitch (nm)	Physical length(nm)		
45	2007	2007 2008	68 59	32 29	14	1.0
35	2009	2009 2010	52 45	27 24	12	0.8
22	2011 2012	2011 2012	40 36	22 20	10	0.6
16	2013 2014	2013 2014	32 29	18 16	?	?

*EOT- equivalent oxide thickness

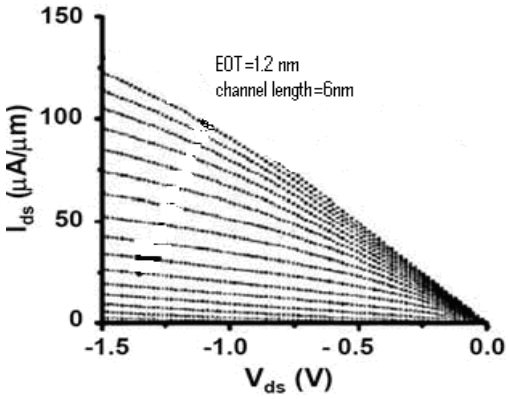


Fig-3. Experimental 6 nm MOS transistor with 1.2-nm thick SiO_2 gate still shows a switch gain Shows the current–voltage characteristics of this transistor [3,5].

2. SCALING LIMIT OF SIO_2

Thirty years ago oxide thickness was 100 nm and now it is 0.7 nm in production while direct tunneling limit of conventional oxide (SiO_2) was 3 nm. The gate oxide up to 0.7 Å has been obtained having only two atomic layer of SiO_2. Further Scaling is difficult [10]. One of the most convincing experiment which demonstrated that 3 nm is fundamental limit [11,15]. Using the scanning transmission electron microscope (STEM) probes and through detailed

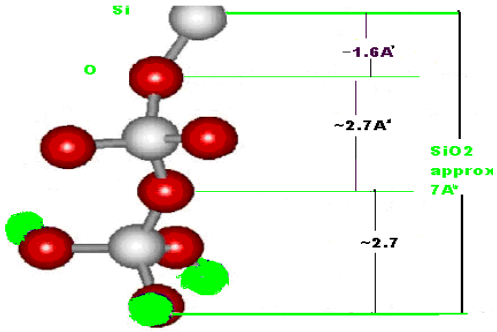
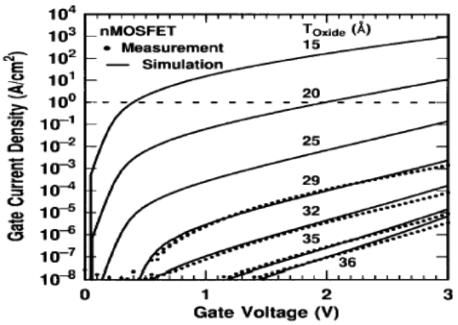


Fig-5 Bonding structure of SiO_2

Electron Loss Spectroscopy (EELS) measurements they studied that device structure and chemical composition of the oxide layer as thin as 0.7-1.2 nm. In the literature work, the local energy gap was given by separation between highest occupy and lowest occupied states. They found that to ensure bulk like bonding for monolayer minimum three or four monolayer of SiO2 were needed. This is the first physical dimension of atomic level. EELS show that the SiO2 thickness must have two layers to show a full gap of 8.9 eV [11]. The few unscalable parameter interface thickness and trap cross section challenges gate dielectric reliability. When oxide is in nanometer even small non-uniformity either in chemical composition or even at surface fluctuation device characteristics 10 fold [12,16] . As scaling fall under two main categories high performance (HP) devices and low performance (LP) devices. HP is used for devices like desktop and server application so high leakage is acceptable while for LP devices like mobile main goal is minimization of power consumption for battery life, this requirement can be fulfilled by introduction of some novel gate dielectric [13,17]. According to Lo et al. reduction in oxide thickness from 2nm to 1.5 nm produces leakage current of two order of magnitude [18]. Such values would not be acceptable for devices which operated by lower voltages. As shown in fig-6 the leakage current density 100A/cm2 at 1.5 V for 1.5 nm oxide thickness is undesirable for low power application. Also leakage current increases exponentially as oxide thickness reduced linearly which is one of the major criteria for future CMOS technology [18]. As the oxide thickness reaches the atomic level further scaling is impossible in nanometer range. Also supply voltage of 1.1 and oxide thickness of 0.9 nm devices does not perform reliably because of large oxide field with further decrease in supply voltage. This happens because part of the applied voltage drops in inversion layer of the channel. So alternative to continue to scaling to SiO2, recent effort has focused on development of alternative dielectric material, whose Si interface properties match the high quality of Si/ SiO2 interface. [19-21].So far the traditional approach followed to scale the gate dielectric has been reduce tox to increase Cox. Where Cox=K SiO2ε0 / tox where K SiO2=3.9. To reduce main problem of tunneling current scaling forces towards high-K dielectric approach relative to SiO2 to increase physical thickness of film (t high-k) with higher values gate capacitance. (C high-k)= (K high-k) ε0/ (t high-k).



- High gate leakage current
- EOT control
- Thermal stability
- Interfacial layer formation
- Channel mobility
- High-k stability with poly-Si-Gates
- Metal Gate electrodes

Fig-8(a) R&D issue for high-k

2.1 ALTERNATE DIELECTRIC MATERIAL:

The choice of thicker class of materials, known as "high-k," may replace today's silicon dioxide technology not for 45 nm or 32 nm but can also be scaled to the end-of-the roadmap technology nodes. Typically for high-k materials under investigation are Al_2O_3[22-26], ZrO_2[27-29], HfO_2[30], Ta_2O_5, TiO_2[31-33], Er_2O_3, La_2O_3, Pr_2O_3, Gd_2O_3[34], Y_2O_3, CeO_2 etc. and some of their silicates such as $Zr_xSi_{1-x}Oy$, $Hf_xSi_{1-x}Oy$, $Al_xZr_{1-x}O_2$ etc. The key guideline for Research and development are given in fig-8(a).

2.2 CHOICE OF HIGH-K MATERIAL:

We may classify them in three main classes, class 1 needs, three basic properties with dielectric constant range 15-25. Band gap about 5 eV behave as insulator. Ferromagnetic materials are less desirable because of their nonlinear electrical response. Polarization of dielectric will have both electronic and ionic components. Because of large -ionic polarization defect formation is easier. Class II The dielectric microstructure may be of amorphous, polycrystalline or epitaxial. However it is important that dielectric should be

- permittivity, band gap, and band alignment to silicon
- Thermodynamic stability
- Film morphology
- Interface quality
- Compatibility with material used in CMOS
- Low leakage current density (<1 A/cm^2 @$V_{GS}=V_{DD}$)
- Reliability comparable to SiO_2
- Low fixed oxide charge / interface state density < 10^{11} cm^{-2}
- Equivalent oxide thickness (E_{OT}) - 10 to 15Å
- Large band gap(> 6 eV) / suitable band off-sets
- High dielectric constant ($10 < \sum r < 50$)

8(b)selection criteria for high-k

Fig-6 Oxide leakage current vs oxide thickness [18]

non-reactive with Si and with gate contacts. Class III needs to relate to performance. The dislocation defects, grain boundaries or point defects related to electrode roughness results to leakage current [36].The ferroelectric class of material having K range 100 to 1000 has been pursued for 1GB and beyond dynamic random access memories (DRAM) storage capacitors [37]. Because of composite structure and stability with adjoining layers can't be used for transistor gate dielectric. Many high-K materials consist of oxide and alloys shown in fig-7 include column 3B material Y2O3, La2O3, column 4B material ZrO2, & HfO2, Column 5B material Ta2O3 have and also approximately inverse relation between band gap and static dielectric constant obeyed by a number of representative high–K dielectrics. It should be noticed that offset energy difference between oxide and silicon valance bonds ΔEv, has same importance as ΔEc for the functioning of oxide in CMOS application. The value of ΔEv can be obtained by knowing the value of ΔEc from the equation Ego-(ΔEc + EgSi), where Ego and EgSi are the band gap values of the oxide and silicon respectively.It has also been observed that d-electron metal transferred nearly its entire valance electron to the oxygen atom, so increased iconicity and have polarization.

The natural vibration frequency associated with metal oxygen bond lowered and highly desirable in microelectronic applications. It is the purpose of the remaining paper to explain complex issues for the use of high-K material for gate dielectric applications and also to provide an update review on Hfo_2, ZrO_2, TiO_2, Gd_2O_3 and some another high-K dielectric material shown in table-4.Aluminum oxide (Al_2O_3) having k value of 10 having problem of large fixed charge and interface trap density hence does not meet our future requirement [39-44]. Lanthanum oxide (La_2O_3) and Lanthanum aluminum oxide ($LaAlO_3$) having dielectric constant ~30 and band gap ~6 eV have thermal stability with temperature up to 850 °C with amorphous nature and main problem of moisture absorption.[45-46]. TiO2 have lowest crystalline temperature of about 400°C for CMOS technology. Problems of fringing field can lower the source channel potential barrier and the threshold voltage [35-36].

Yttrium oxide (Y2O3) has problem of high interface density >1012 eV-1cm-2 , low crystalline temperature, and formation of silicide and silicate [47]. The leakage current of ZrO2 and HfO2 found to be 4-5 order of magnitude lower than SiO2 of equivalent gate oxide thickness. HfO2 films behave reported quite similar to ZrO2 because of similar fabrication chemistry and material properties. Hafina & Zirconia are less stable then their silicates, so Hafnium and Zirconium silicate films were examined for electrical properties. The films were prepared by plasma enhanced Chemical Vapor deposition (PECVD) method. The samples having a metal insulator semiconductor structure were examined. The permittivity value was found 7 double of SiO2 and dielectric film operated at 10MV/Cm. Conduction band offset of ZrO2 may be 0.8 t0 1.2 eV which is too low for MOS gate dielectric. While oxinitride having higher dielectric and stability values with slightly poor characteristics can be used down 25 nm technology node. Among the rare earth oxide Gd2O3 Gadolinium oxide has various features listed in table-3 and table-4. Verify that it can be used as high-K applications. The leakage current density of Gd2O3 films decreased for RTA(rapid thermal annealing) in N2 and increased in O2. The interface and structure of the Gd2O3/Si was amorphous and both cubic and monoclinic phases were well oriented. Further research work is required to improve electrical properties of high-k material thin films

Fig 7. Part of periodic table. Illustrated in boldface are the elements which cations (with electronic structure of active states in the second line), can combine with an anion (in italic) to form an insulating oxide.[7]

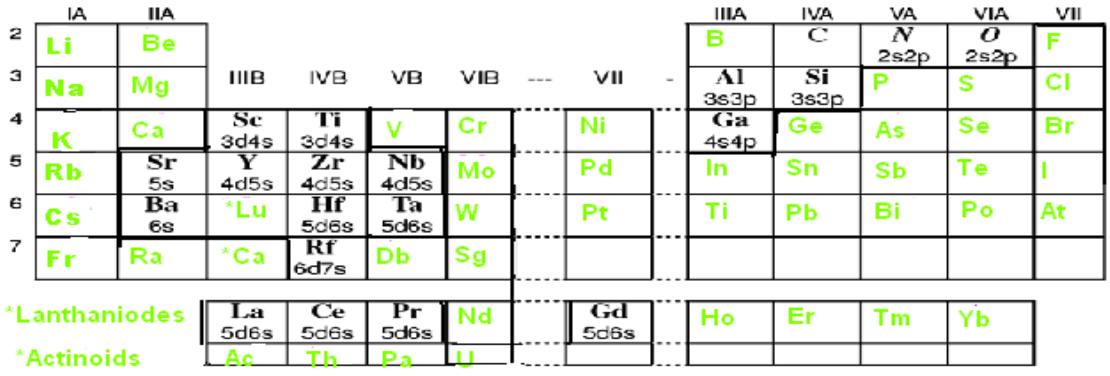


Table-3 List of rapidly expanding material in CMOS technology [38-43]

Material	Dielectric Constant (K)	Band gap (E_g) (eV)	Conduction Band Offset ΔE_C (eV)	Valence Band Offset ΔE_V (eV)	Stability With Si	Crystal Structure
Silicon	3.9	8.9	3.5	4.4	yes	Amorphous

dioxide (SiO_2)						
Silicon nitride (Si_3N_4)	7.0	5.1	2.4	1.8	Yes	Amorphous
Aluminum oxide (Al_2O_3)	9.0	8.7	2.8	4.9	Yes	Amorphous
Gadolinium oxide (Gd_2O_3)	12	5.4	3.2	3.9	Yes	Amorphous
Yattrium oxide (Y_2O_3)	15	5.6	2.3	2.6	Yes	cubic
Zirconia (ZrO_2)	25	7.8	1.4	3.3	Yes	Monoclinic, cubic, tetragonal
Tantulum pentoxide (Ta_2O_5)	26	4.4	0.3	3.1	No	orthorhombic
Hafnia (HfO_2)	25	5.7	1.5	3.4	Yes	Monoclinic, cubic, tetragonal
Lanthana (La_2O_3)	30	6	2.3	0.9	Yes	Hexagonal, cubic
Titanim oxide (TiO_2)	80	3.5	1.2	1.2	yes	Tetragonal
Strontium titanate ($SrTiO_3$)	300	?		?	no	cubic

Table 4- Comparisons of properties of hafnium, Zirconium, Titanium, & Silicon Oxide, Gadolinium oxide , EOT calculated for oxide thickness of approximately 30nm film. Electrical characteristics by considering T=300K, standard physical constant (q,K,Є0), electrode area $1*10^{-2}$ $cm^{-2.}$

Properties	**SiO_2**	**HfO_2**	**ZrO_2**	**TiO_2**	**Gd_2O_3**
Structure	Amorphous	Non-crystalline	Nano-crystal	Amorphous, Rutile	Amorophous
Dielectric Constant	3.9	20-25	22-26	22-40	23
Band gap (eV)	8.9	5.6	4.7-5.7	3.2	5.4
Technological					
Formation Temp.(°C)	>700	350	350	400	550
Silicide formation	NA	Yes	Yes	NA	No
Thermal Stability	1000	950	900	550	1200
Electrical (approximat values**)**					
Interface trap density ($eV^{-1}Cm^2$)	10^{10}	10^{12}	10^{12}	10^{12}	10^{10}
Oxide trap density (Cm^{-2})	10^{11}	10^{12}	10^{12}	10^{12}	10^{11}
Breakdown field (MV/Cm)	10	<4	<4	<4	3.5
Capacitance (C_{ox}) F/Cm^2	$4.67*10^{-9}$	$6.49*10^{-7}$	$6.79*10^{-7}$	$8.85*10^{-7}$	$4.67*10^{-9}$
Flat band voltage (V_{fb}) V	4.15	0.85	0.25	.25	.23
Threshold Voltage (V_t) V	4.9	1.48	0.88	.86	.85
Bulk Potential($Ø_f$)	.30	.30	.30	.30	.30
EOT nm	1100	35.45	33.99	31.15	33.74
Low Leakage current density wrt SiO2 (A/Cm^2)		10^4-10^5	10^4-10^5	10^1-10^2	10^2-10^3
Properties	**SiO_2**	**HfO_2**	**ZrO_2**	**TiO_2**	**Gd_2O_3**
Structure	Amorphous	Non-crystalline	Nano-crystal	Amorphous, Rutile	Amorophous
Dielectric Constant	3.9	20-25	22-26	22-40	23
Band gap (eV)	8.9	5.6	4.7-5.7	3.2	5.4

Technological					
Formation Temp.(°C)	>700	350	350	400	550
Silicide formation	NA	Yes	Yes	NA	No
Thermal Stability	1000	950	900	550	1200
Breakdown field (MV/Cm)	10^{10}	10^{12}	10^{12}	10^{12}	10^{10}
Capacitance (C_{ox}) F/Cm^2	10^{11}	10^{12}	10^{12}	10^{12}	10^{11}
Flat band voltage (V_{fb}) V	10	<4	<4	<4	3.5
Threshold Voltage (V_t) V	$4.67*10^{-9}$	$6.49*10^{-7}$	$6.79*10^{-7}$	$8.85*10^{-7}$	$4.67*10^{-9}$
Bulk Potential($Ó_f$)	4.15	0.85	0.25	.25	.23
EOT nm	4.9	1.48	0.88	.86	.85
Low Leakage current density wrt	.30	.30	.30	.30	.30
SiO2 (A/Cm^2)	1100	35.45 10^4-10^5	33.99 10^4-10^5	31.15 10^1-10^2	33.74 10^2-10^3

Table-5 comparison of various MOS capacitor with different dielectric material and their leakage currents [34,50]

Capacitor	Gate dielectric	Dielectric constant	EOT(nm)	Leakage current density V= 1V(A/Cm^2)
1	TiO_2 (58nm)	40	5	0.07
2	TiO_2(58nm)/ SiO_2(6nm)	20	12	$4.7x10^{-6}$
3	SiO_2 thermally grown grown	3.9	5	$<10^{-9}$
4	SiO_2 (49nm)	3.9	49	$1.3x10^{-8}$
5	Gd_2O_3(15nm)	23	2.3	3.6×10^{-5}
6	ZrO2	7		3.25×10^{-5}
7	HfO2	10		4.1×10^{-6}

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4. CONCLUSION:

The high-K alone can't be a feasible solution for future CMOS technology. System on Chip (SoC) and System in Package (SiP) technologies provide a path for continous improvement in performance, power, cost and size at the system level. As we have reached the below .7 nm in scaling. So it is difficult to continue with the historical trend of scaling. So there is need of innovations in the field of advanced material, non planar device structure, process control, manufacturability, and leakage current. To continue the conventional path of scaling there is need high-K material with suppressed tunneling current, higher channel doping for reducing short channel effects, trade off between mobility degradation and increased leakage power consumptions. The scaling below 16 nm is attainable by alternate to replace Si and alternate to replace new information technology to replace CMOS. The La_2O_3 have serious reliability problems for the actual application for MOS gate dielectric. It can also be concluded that the Gd_2O_3 films grown by magnetron sputtering may be promising candidate as high-K gate dielectric in CMOS devices. Hafnium oxide and Zirconium oxide have shown much promising properties to replace SiO_2. TiO_2 and other high-k material have basic problem is variation in threshold voltage due to both oxide traps and interface trap generations. So it can be concluded that the high-k materials, along with the right process recipe, may reduce gate leakage, for delivering expected transistor performance.

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