Abstract

Pipelining is used for increasing the throughput of the system. Wave pipelining is done by removing the intermediate registers present in the pipelined circuits so that there will be only an input register and an output register. Circuit should be modelled in such a way that all data from one stage should reach the next stage at the same time so that overlapping of data will not occur. In wave pipelined system the clock period should be greater than the difference between maximum delay and minimum delay + clocking overheads such as setup time, hold time, etc. Clock period can be reduced by minimizing the difference between maximum and minimum delay, i.e delay equalization has to be done. Delay equalization can be done by logic restructuring combined with Wong’s algorithm and Klass’s algorithm. Area can be further decreased by using delay element shifting and delay element sharing.

Reference

- Srivastav Sethupathy, Nohpill Park, Marcin Paprzycki, “Logic restructuring for delay balancing in wave-pipelined circuits: an integer programming approach”, in proceedings of the seventh international symposium on symbolic and numeric algorithms for scientific computing, 2005 IEEE.

Index Terms

Electronics System Architecture

Key words

Wave pipelining Delay equalization Logic restructuring Delay element sharing and shifting