Abstract

The appropriate choice of flip-flop topologies is of essential importance in the design of integrated circuits for CMOS VLSI high-performance and high-speed circuits. The understanding of the suitability of the flip-flops and select the best topology for a given application is important to meet the need of the design to meet low power and high performance circuit subject. This work shows a wide area comparison exist in D flip-flop, this provides a wide study of the topologies in terms of power dissipation, delay, and rise delay and fall delay time.

References

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Keywords

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