Abstract

The appropriate choice of flip-flop topologies is of essential importance in the design of integrated circuits for CMOS VLSI high-performance and high-speed circuits. The understanding of the suitability of the flip-flops and select the best topology for a given application is important to meet the need of the design to meet low power and high performance circuit subject. This work shows a wide area comparison exist in D flip-flop, this provides a wide study of the topologies in terms of power dissipation, delay, and rise delay and fall delay time.

References

- Haiqing Nan and Ken Choi "High Performance, Low Cost, and Robust Soft Error
- Pedro M. Figueiredo &quot;Comparator Metastability in the Presence of Noise&quot; IEEE Transactions, on circuits and Systems I: Regular Papers year 2012 pp no 1549.

Index Terms

Computer Science Circuits And Systems

Keywords

Metastability D Latch Flip-Flop Microwind.