Abstract

In real time applications, most of the times, image is subjected to the noise due to the transmission of images through the channels, scanning, digitizing, and storing at the output. If this noisy image is used for the further processing, it may leads to the incompetent decision for the human interpretation. So the image filtering is essential to keep away from the noise present in the image. The performance of an image filtering system depends on its capability to detect the occurrence of noisy pixels in the image. The earlier image filtering methods has a drawback of pure image quality i.e. low PSNR and high MSE values. And also these filtering methods are designed using PC. Generally PC based image filtering system uses general purpose processor. This type of implementation takes more amount of time to provide the filtered result. Because this PC based filtering system executes the instructions in step by step manner. In order to eradicate the drawbacks associated with existing filtering methods, a new filtering technique is implemented by means of FPGA. Because FPGA’s supports parallelism. This new proposed technique gives high image quality that means High PSNR and low MSE values. And also this FPGA based hardware implementation takes less amount of time to get the filtered result.
Hardware Implementation of Modified Weighted Median Filtering on FPGA

References


Index Terms

Computer Science

Image Processing
Keywords
    Image noise FPGA PC PSNR MSE