Abstract

We can use a high-speed parallel adder in incrementer / decrementer to improve the operating speed which can count up or count down from the loaded value by one step in one clock cycle. For this, design of a faster and highly reliable adder is of major importance. Thus, much effort has been invested in the research that has led to faster and more efficient ways to perform this operation. To prove the efficiency of the proposed method, the circuit is simulated in pass transistor CMOS 50nm technology and some simulation parameters are calculated in the layout of the circuit. The binary decrementer reduces the stored binary data in memory or register by 1. This can be done by using 2's complement method by using XOR gates which convert binary data in 1's complement and then by addition of binary 1; it can be converted to 2's complement form. It is made by cascading full adders for number of bits i.e. the storage capacity of the register to be decremented. Hence, a 4-bit binary decrementer requires 4 cascaded half adder circuits. This paper presents the eight bit CMOS base incrementer and decrementer logic design using eight bit adder and subtractor. The parametric simulation is done on MICROWIND layout editor tool. The any conventional static CMOS adder with pullup and pulldown logic
Transmission Gate base Programmable Binary Incrementer Decrementer

requires 32 MOSFET whereas our design adder requires 30 MOSFETs. Our design methodology is based on static CMOS logic and transmission gate logic to achieve smaller delays, reduce power dissipation and optimized area.

References

- Itamar Levi, Alexander Fish "Dual Mode Logic Design for Energy Efficiency and High Performance"; IEEE access

Index Terms

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Keywords

Incrementer/ decremnter Layout design Transmission gate