Abstract

Speed improvement in Digital signal processing is considered to be challenging. High speed multipliers and adders are prime requirement for digital filters and for FFT operations. Vedic mathematics is an ancient scheme based on 16 formulas (sutras). These are simple and easy methods which can be directly applied for DSP computations. Many researchers have worked on multiplier designs using Vedic operators. Present paper deals with exhaustive review of literature based on Vedic mathematics. It shows that Vedic mathematics can be used for fast signal processing. Multipliers based on Vedic mathematics can be used for speed improvement, reduction in power consumption, complexity, area etc. Vedic mathematical algorithms can be proved efficient over traditional (existing) methods in FIR and IIR filters for providing effective results in de-noising of biomedical Signal.

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Index Terms

Computer Science  Signal Processing

Keywords

Vedic Mathematics  Multiplier  DSP  Filter Design