Abstract

Different adder circuits are elementary blocks in many contemporary integrated circuits, which are not only employed to perform addition operations, but also other arithmetic operations such as subtraction, multiplication and division. Full adder is the basic building block of any adder circuit. Area, speed and power are the three main design metrics for any VLSI circuit. In this work, eight different full adders’ circuits based on standard (std.) CMOS, CPL, 16-Transistor, DCVSL, PTL, TGA, 14-Transistor and 8-Transistor have been designed and implemented using Tanner EDA simulation tool. In this paper, authors have compared the propagation delay, power consumption and power delay product (PDP) of different full adder circuits by varying supply voltage (Vdd).
References


Index Terms
Computer Science  Circuits And System

Keywords
CMOS full adder  Propagation delay  PDP  DCVS  PTL  Tanner EDA tool.