Abstract

Different adder circuits are elementary blocks in many contemporary integrated circuits, which are not only employed to perform addition operations, but also other arithmetic operations such as subtraction, multiplication and division. Full adder is the basic building block of any adder circuit. Area, speed and power are the three main design metrics for any VLSI circuit. In this work, eight different full adders have been designed and implemented using Tanner EDA simulation tool. In this paper, authors have compared the propagation delay, power consumption and power delay product (PDP) of different full adder circuits by varying supply voltage (Vdd).
Relative Performance Analysis of Different CMOS Full Adder Circuits

References

Relative Performance Analysis of Different CMOS Full Adder Circuits


**Index Terms**

Computer Science  

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**Keywords**

CMOS full adder  Propagation delay  PDP  DCVS  PTL  Tanner EDA tool.