High Speed Architecture for KECCACK Secure Hash Function

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Abstract

Cryptography is a technique that protects the information, which is in transit or in storage, from unauthorized or unexpected reveals. This paper demonstrates a Secure Hash Algorithm-3 (SHA-3) called Keccak, and also proposed a hardware architecture for the Keccak to support high speed security application. Since SHA-3 supports high level of parallelism, the proposed hardware architecture brings higher speed, in terms of bit rate and capacity, and also provides better security demanded by Internet of Things. This paper also demonstrates the architectural attributes of popular and real life cryptography techniques such as, Secure Hash Algorithm-1 (SHA-1), Secure Hash Algorithm-2 (SHA-2) and Advanced Encryption Standard (AES). In this research, the security techniques AES, SHA-1, SHA-2 and SHA-3 has been implemented on Virtex-5 FPGA device and their architectural attributes were captured. Finally, the proposed architecture of SHA-3 is compared with architecture of contemporary security techniques (AES, SHA-1, and SHA-2) in terms of speed, area and power. The comparison results shown that the SHA-3 architecture brought optimum performance over its contemporary security techniques.
References

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Index Terms

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Keywords

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