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## Abstract

Networks-on-Chip (NoCs) are increasingly used in many-core architectures. Today's technology for ASICs supports Networks-on-Chip designs which can have 100 million gates on a single chip. In order to implement a competitive NoC architecture in FP-GAs, the area occupied by the network should be kept to a minimum. This helps in utilizing maximum area by the logic while maintaining the performance of the router network. Reducing area also reduces the power consumption. NOC's designs promise to offer considerable advantages over the traditional bus-based designs, in solving the numerous technological, economic and productivity problems associated with billion-transistor system-on-chip development. Here, a very flexible network is designed to propose a highly scalable and can be easily changed to accommodate various needs. This proposed work focused on implementation, analysis and verification of a five port routers. The building blocks of the router are input/output, multiplexer/demultiplexer, crossbar switch, buffer register and arbiters. The arbiters uses the round robin algorithm. The proposed NOC architecture is simulated in Xilinx ISE10.1 software. The source code is written in VHDL. This design is suitable for building networks with irregular topologies and with low latency and

high throughput.

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### Index Terms

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### Keywords

NOC, VHDL, Router Architecture

