Abstract

In this paper, an FPGA based FIR filter for Satellite Application is presented. The implementation is based on Factored Canonic signed digit (FCSD) which eliminates the use of embedded multipliers. The FIR filter has been implemented using Equiripple on an FPGA. In Equiripple, the ripples are distributed more evenly over pass band and stop band which results in a better approximation of desired frequency response can be achieved. The digital band pass filter used in satellite uplink model which is located before up converter. The uplink model used here is for C band small satellite communication system. With the performance evaluation of the equiripple filter design, it is found to be the most suitable and optimized method to meet the desired specification uplink model. An 89 tap FIR filter has been designed and simulated using 16 bit input and output precision in MATLAB environment. The behavioral simulation of VHDL model has been performed using ISE simulator. The simulated model has been synthesized using Xilinx synthesis tool (XST) on SPARTAN 3E based 3s500efg320-4 and Virtex 2P based 2vp30ff1152-5 target FPGA devices. The results depicts that FIR filter on Virtex 2P is 22.46% faster the SPARTAN 3E.
References


Index Terms

Computer Science

Signal Processing

Keywords
FCSD, FIR, uplink, FPGA, MATLAB