Abstract

An efficient high throughput FIFO (First-In-First-Out) system using GALS (Globally Asynchronous Locally Synchronous) technology is designed for data transfer from one domain to another domain with the development of a modeling and simulation framework whose results are obtained as RTL (Register-Transfer Level) Schematic. Integration of several of IP (Intellectual Property) cores into a single chip in order to fulfill the demand of latest applications, leads to various timing issues especially interfacing between the different clock domains. The GALS technology provides a clock distribution feature for the same. A general purpose 8-bit synchronous core design favoring the GALS technology is used for the designing. The model is implemented in VHDL (Very High Speed Integrated Circuits Hardware Description Language) with Xilinx ISE (Integrated Synthesis Environment) Design Suite 14.5 Version software and simulated using ISim tool. The synthesis results show improved throughput and reduced chip area using GALS.

References
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Index Terms

Computer Science
Circuits and Systems

Keywords

FIFO (First-In-First-Out), GALS (Globally Asynchronous Locally Synchronous), RTL (Register-Transfer Level) Schematic, System-On-Chip (SoC), IC (Integrated Circuit),
throughput, chip area.