Abstract

This paper presents asynchronous switch between any two different local clock synchronous domains. The asynchronous switch will generate a slower clock from two local clock modules and moderate the high rated clock domain to slow down its clock frequency without stopping or pausing any clock of them throughout the data communication among them. The proposed design is implemented using the CMOS 45nm technology of STMicroelectronics. In this case, the delay time to change the clock is shown to be about 0.4ns. The proposed system is designed to use a small number of circuit elements. So that, the asynchronous switch has a noticeable improvement in terms of power consumption, throughput, and circuit area.

References

Design of a Self-Timed Data Synchronizer for Crossing Two Different Clock Domains


Index Terms

Computer Science  Circuits and Systems
Keywords

SOC, GALS, FIFO, PSTR