Abstract

As the compactness of system-on-chip (SoC) increase, it becomes striking to integrate dedicated test logic on a chip. Starting with a broad idea of test problems, this survey paper focus on “Chip” Built in Self-Test (BIST) study and its promotion for board and system-level applications. This paper gives brief informative review of Built-in Self-test (BIST) and its testing techniques. Recently BIST Research is being highly used in VLSI and SoC testing for the detection fault coverage.

References

concurrent BIST with Low hardware overhead.”
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Index Terms
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Built-in Self-test, Circuit under test, Device under test, IC, SOC, CTL, PRNG, CRC.