Abstract

The urge of high performance and dynamic functionalities in an integrated circuit has led to aggressive technology scaling over the years. The supply voltage (VDD), device threshold voltage (Vth) and the device geometry are expected to be scaled further with this trend. Which results in reducing the short channel effects and increased transistor OFF-state current (IOFF). Additionally leakage currents, higher operating frequency and on die transistor count will lead to increase in total power dissipation. Dynamic logic technique is preferred over static logic technique for the higher performance circuit due to lesser delay which enhances the speed of the circuit and overall capacitance is low compare to CMOS which reduces the power consumption. In this paper we have calculate the Average power consumption and delay of various domino circuits provided with 8 input OR gate, comparison of power, delay, and Unit Noise Gain (UNG) of different topologies. The simulation is performed in HSPICE at 65nm and 45nm process technology with supply voltage 1V and 0.9V and operating temperature of 27° C at 100 MHz for fair comparison of results. We have also calculated the power consumption and delay with the variation of keeper ratio in all the existing technique at 65nm and 45nm process
technology.

References


Index Terms
Keywords

Domino Logic, High speed, Low power, UNG