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Abstract

As technology scales down below 65nm there is a rapid growth in semiconductor industries; reduction in transistor size leads to exponential increase in power consumption in DSM technology. The major concerns of VLSI designers are to develop a circuit which is having high performance with minimal size earlier. The fast growth in portable computing and wireless communication has led to the power dissipation along with heating. In this paper we have implemented a novel leakage reduction technique known as Diode switch (Combination of PMOS and NMOS sleep transistor) and inserted a sleep transistor above PUN and below PDN which increases the resistance of the circuit. By inserting the sleep transistor short circuit power consumption reduces which rail the circuit from supply voltage, but there is penalty of area take place. All the simulation is performed 32nm technology by using HSPICE simulator. Proposed DHS circuit reduce 48.98%, DFS reduces 52.89% and DHFS reduces upto 68.27% of leakage power.

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Index Terms

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Leakage Reduction, High speed, Low power, DSM