Abstract

In this paper we have proposed a look-up-table (LUT) based structure for high-throughput implementation of multilevel lifting DWT. The proposed structure can process one block of samples to achieve high-throughput rate. Compared with the best of the similar existing structure, it does not involves any multipliers but it requires more adders and 21504 extra ROM words for J=3; its offers less critical path delay as compared to exiting structure. Synthesis results show that proposed structure has less ADP 56% less area and 13% less power compared to existing structure for block size J=2. Similarly proposed structure has 64% ADP and less power 21% as compared to existing structure for J=3. The proposed structure is fully scalable for higher block-sizes and it can offer flexibility to derive area-delay efficient structures for various applications.

References


**Index Terms**

Computer Science  Signal Processing
Keywords

Look up table (LUT), VLSI, lifting, 2-dimensional (2-D) DWT.