Clock Power Optimizations in VLSI design at Advanced Technology Nodes

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Abstract

Power reduction in VLSI designs is one of the key design constraints along with others, namely timing, area, quality constraints, noise, etc. Even though there has been a steady growth of devices that are able to be placed in a given area of a chip as per Moore’s law, the same cannot be said for battery technologies as they have never been able to catch up. Since the advent of the deep sub-micron era, speed and higher frequency of operation have become the prime goals of any design as the hunger for faster and better optimized systems are never ending. But as a consequence of faster operating speeds which basically means higher clock frequencies, power becomes one of the main constraints to be considered as the most important component of power dissipation, namely the dynamic power dissipation has a proportional relationship with the clock frequency. Hence clock power optimization is taken up as the prime objective of this paper for technologies below 14 nm as at these technologies, other secondary power dissipation components start to become more prominent. Various design techniques have been discussed and applied at both the circuit design and the RTL levels of abstraction in order to provide a complete review of most of the low power design techniques which can be used to
reduce power at both these levels of abstraction. An improvement of 25% and 15.7% of power reduction are observed in clock power and overall power respectively. There is also a power reduction of 2-5% for each of the RTL level optimization techniques.

References

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Index Terms

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Keywords

Activity factor, Clock tree, Clock gating efficiency, Data aware clock gating efficiency, low activity non enabled register, Regional clock buffer, Local clock buffer.