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Abstract

The use of Static Random Access Memory (SRAM) based Field Programmable Gate Array (FPGA) in critical applications has been considered a solution in space and avionics domain due to its flexibility in achieving multiple requirements such as re-programmability and good performance. However, SRAM-based FPGAs are susceptible to radiation induced Single Event Upset (SEU) that affects the functionality of the implemented design. Therefore, an improved Frame Level Redundancy (FLR) algorithm that uses Cyclic Redundancy Check (CRC) as an error detection technique for configuration memory scrubbing, is developed as a solution to mitigate SEU through upset detection and correction. Fault injection was performed on FPGA configuration memory frames on different number of modules to emulate SEU. The improved FLR algorithm was implemented and system level simulation was carried out using MATLAB. The performance of the improved FLR algorithm was compared with that of the existing FLR algorithm using error correction time and energy consumption as metrics. The results of this work showed that the improved FLR algorithm produced 31.6% improvement in error correction time and 61.1% improvement in energy consumption over the existing FLR algorithm.

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Index Terms

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Keywords

FPGA, SRAM, Scrubbing, FLR, SEU, configuration memory, logic bit(s).