Abstract

There is a growing interest in multi-bit Error Correction Codes (ECCs) to protect SRAM memories. This has been caused by the increased number of multiple errors that memories suffer as technology scales. To protect an SRAM memory, an ECC has to be decodable in parallel and with low latency. Among the codes proposed for memory protection are Orthogonal Latin Square (OLS) codes that provide low latency decoding and a modular construction. It is more effective to provide different degrees of error correction for the different bits. This is done with Unequal Error Protection (UEP) codes. In this paper, UEP codes are derived from Double Error Correction (DEC) Orthogonal Latin Square (OLS) codes. The derived codes are implemented for an FPGA platform to evaluate the decoder complexity and latency. The Proposed encoder and decoder are done by Verilog HDL and Simulated by ModelSim 6.4 c and synthesized by Xilinx tool.


**Index Terms**

Computer Science Circuits and Systems

**Keywords**

UEP codes, OLS codes, SEC-DED codes, OS-MLD codes