Abstract

In this paper we are comparing the FIR filters by distributed arithmetic (DALUT) design using sharing lookup table and reconfigurable implementation of distributed arithmetic (RIDA) method. DA-based design with look-up table (LUT)-sharing technique for the computation of filter outputs and weight-increment terms of block least mean square BLMS algorithm. Besides, it offers significant saving of adders which constitute a major component of DA-based structures. While in the reconfigurable implementation of distributed arithmetic (DA) for post-processing applications is described. The input of DA is received in digital form and its analog coefficients are set by using the floating-gate voltage references. This is a major advantage of the DALUT structure for reducing its area delay product (ADP); particularly, when a large order adaptive digital Filter (ADF) is implemented for higher block-sizes.

References


Index Terms

Computer Science Circuit Systems

Keywords

FIR Filter, Distributed Arithmetic (DA) Technique, Look Up Table (LUT), Multiply and Accumulate (MAC).