Abstract

In today’s world scenario more than 85-90% of the chip area is mainly occupied by memory. There is a need for faster and reliable memory system for various integrated devices from computers to various handheld devices. The memory devices such as SRAM, DRAM etc. were served by the traditional MOSFETs till to date but as the demand of the better performing and the compact modeling of the integrated devices are causing the failure of MOSFETs operations. The MOSFET scaling is suffered by Short Channel Effects (SCE’s). SRAM is one of the memories mainly used in the cache memory of devices. It must be faster, less power consuming and reliable but this is affected by CMOS scaling causing process variations. Here in this paper the alternate solution to the issues faced by MOSFET based SRAM is overcome by FinFET based SRAM. A 6T short gated FinFET based SRAM is taken for the study and the spice models are created at 22nm and 14nm using Predictive Technology Models (PTM) and simulated using HSPICE. The performance is analyzed in terms of Static Noise Margin (SNM), power and delay for the 6T SRAM. The results shows FinFET based SRAM is faster, reliable and the power consumption is significantly reduced and offers good trade-offs at lower
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technology nodes.

References

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Index Terms

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Keywords

SRAM Cell, FinFET, CMOS, SNM, PTM Read delay, Write delay