A Novel Systolic Array Architecture for Matrix Multiplication Circuit Design using Carbon Nanotube Technology

International Journal of Computer Applications
Foundation of Computer Science (FCS), NY, USA

Volume 172 - Number 6

Year of Publication: 2017

Authors:

Alireza Azimian, Ali Kargaran Dehkordi, Mohammad Tehrani

10.5120/ijca2017915156

Abstract

Recently, parallel computing has been considered increasingly and many researchers have focused on this topic in order to enhance their designs, especially speed parameter to reach lower delay in computational operations. Among the methods which use parallel computing, systolic arrays have attracted researcher’s attention because of its unique characteristics. Systolic arrays are arrays of processors which are connected to a small number of nearest neighbors in a mesh-like topology. Processors perform a sequence of operations on data that flows between them. Generally the operations will be the same in each processor, with each processor performing an operation (or small number of operations) on a data item and then passing it on to its neighbor. Systolic arrays are often using for specific operations, such as "multiply and accumulate", to perform massively parallel integration, convolution, correlation, matrix multiplication or data sorting tasks. On the other hand, silicon limitations for transistors fabrication in future causes a need to substitute this technology by an appropriate ones that among them carbon nanotube (CNT) technology has the most probability. In this paper we
conducted a survey on using systolic array in multiply and accumulate operations by a VLSI circuit based on CNT technology.

References


Index Terms
Keywords

Systolic Array; Parallel, CNT, Matrix Multiplication, CMOS, Cell.