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Abstract

In wide fan-in domino multiplexors, significant power losses are introduced due to the high switching activity at both dynamic and output nodes. In this paper a multiplexor is proposed with static switching at both dynamic and output nodes. This technique has a control pulse generator circuit which turns on the pull up transistor conditionally for a short duration only. This technique is advanced than previously existing techniques as it has faster response over other existing techniques but lesser power consumption and lesser area required. Simulation is done using 0.18µm CMOS technology. Power consumption of proposed multiplexor is calculated and the results are compared with existing multiplexors for different loading condition, clock frequency and temperature. For capacitance 100 fF, proposed domino multiplexor circuit reduces power consumption by 81.08%, 17.57% and 25.50% as compared to standard footless domino, SP-Domino and SSPD multiplexors.

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Index Terms

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Keywords

Multiplexor, Domino logic, Dynamic circuits, Low power, Switching activity.