Abstract

Reliability of on-chip communication became a challenge in deep submicrometer (DSM) region due to the increased effect of the different noise sources and the crosstalk between adjacent interconnects. This led to the introduction of many coding schemes to jointly address both issues. In this paper, high error detection with single error correction joint coding scheme is proposed. The proposed scheme limits its error correction to single error as it was found that this meets the performance requirements while allowing the scheme to detect higher number of errors, namely six errors in this proposed scheme. The proposed scheme was implemented in two different designs, one optimized for higher performance and the other for smaller area. The two designs were evaluated and compared to similar coding schemes. The scheme achieved higher reliability and maintained high throughput. As compared to previous work, the first implementation achieved 4% higher frequency whereas the second implementation achieved 13% smaller area and 11% lower power.


Crosstalk Aware Multi-Bit Error Detection with Limited Error Correction Coding for Reliable On-Chip Communication

Index Terms

Computer Science  Communications

Keywords

Error control, fault tolerance, network on chip