Design of IIR Systolic Array Architecture by using Linear Mapping Technique

Abstract

Design of IIR (infinite impulse response) systolic array architecture by using linear mapping technique is proposed in this paper. Systolic array architecture maps high level computations into hardware structures. In a systolic array, all the processing elements (PEs) are uniform and fully pipelined. On regular dependence graph, systolic architectures are designed by using linear mapping techniques. IIR filters are used in digital signal and image processing applications. IIR filters are recursive filters. IIR filters have high selectivity and less number of coefficients than the FIR (finite impulse response) filters. Various IIR systolic arrays architectures such as design B1, design B2, and design F is proposed in this paper. By selecting the projection vector, processor vector and scheduling vector these designs are derived.

References

1. H.T.Kung and C.E.Leiserson, “Systolic arrays (for VLSI),” in Sparse Matrix Symposium,
Design of IIR Systolic Array Architecture by using Linear Mapping Technique


Index Terms

Computer Science

Circuits and Systems

Keywords

Systolic array, DG, PEs, FIR, IIR, DSP