In recent years, Quantum Electronics and Reversible Logic have emerged as a major area of research having applications in low power CMOS circuits, cryptography, optical computing and nanotechnology. The fact that classical logic gates such as AND, OR, XOR etc., barring the NOT gate, cannot predict the input given the output and hence generate heat due to information
loss, has given rise to the concept of reversible logic. In this paper, a new reversible 4 * 4 “SCG” gate has been proposed which is being used to realize the classical set of logic gates in the reversible domain. The most promising fact of the proposed gate is that a single SCG gate can be used to realize a reversible Full Adder/Subtractor circuit or a single bit reversible Comparator. It has been shown that the Full Adder/Subtractor and the single bit Comparator using the proposed gate is much better and optimized in terms of number of garbage outputs and the number of reversible gates used in comparison to the existing counterparts in literature. Further efficient Reversible Parallel Adder/Subtractor circuits and Match Logic have been designed using the proposed SCG gate. Also a 4-bit digital comparator has been designed by cascading a series of single bit comparators using SCG gate.

Reference

- H. Thapliyal and M.B Srinivas, “A New Reversible TSG Gate and Its Application For

Index Terms
Computer Science
System Architecture

Key words
Reversible Logic
Reversible Gate
Reversible
Full Adder/Subtractor
Reversible Comparator
Garbage Output
Constant Input
Match Logic