Abstract

The explosive growth of battery operated devices has made low-power design a priority in recent years. Moreover, embedded SRAM units have become an important block in modern SoCs. Present day SRAMs are striving to increase bit counts while maintaining low power consumption and high performance. To achieve these objectives there is a need of continuous
scaling of CMOS transistors, and so the process technology scaling and need for better performance enabled embedding of millions of Static Random Access Memories (SRAM) cells into modern-day ICs. In several applications, the embedded SRAMs can occupy the majority of the chip area and contain hundreds of millions of transistors. As the process technology continues to scale deeper into the nanometer region, the stability of embedded SRAM cells is a growing concern. The supply voltage must scale down accordingly to control the power consumption and maintain the device reliability. Scaling the supply voltage and minimum transistor dimensions that are used in SRAM cells challenge the process and design engineers to achieve reliable data storage in SRAM arrays. This task is particularly difficult in large SRAM arrays that can contain millions of bits. In this paper we proposed a novel 9T SRAM cell with the objective to increase the stability and reduce the leakage for multimedia mobile applications at deep submicron level. All the Simulations are done at 45nm technology.

Reference


**Index Terms**

Computer Science  
Integrated Circuits

**Key words**

SOCs.  
Scaling  
Deep submicron  
level  
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SRAM
Characterization of PNN Stack SRAM Cell at Deep Sub-Micron Technology with High Stability and Low Leakage for Multimedia Applications