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International Journal of Computer Applications
© 2011 by IJCA Journal

Volume 35 - Number 8

Year of Publication: 2011

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10.5120/4419-6140

{bibtex}pxc3976140.bib{/bibtex}

Abstract

Cholesky factorization is the computationally most expensive step in numerically solving positive definite systems. Due to inherently recursive computation process and associated

floating point division and square root operations in Cholesky factorization, it is very difficult to obtain acceleration by exploiting parallelism on FPGA's. To solve this problem, approach suggests iterative architecture with parallelly fetching the matrix elements using customized Diagonal Processing Elements (DPU), Non Diagonal Processing Elements (NDPU) and Triangular Processing Elements (TPU) as computational processing units. The use of LNS approach using LUT technique for floating point square root and division arithmetic eventually improves resource and clock cycle utilization. Scheme is implemented using Xilinx Virtex-4 FPGA and achieves 0.032 μ s clock latency and obtained a throughput of 31.25Mupdates/s operating at 125 MHz for 4x4 matrix inversion problem.

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Index Terms

Computer Science

Integrated Circuits

Keywords

Architecture

Cholesky Factorization

FPGA's

Iterative

Virtex-4

