Abstract

Steganography is the art of hiding information in a cover medium such that the existence of information is concealed. An image is a suitable cover medium for steganography because of its great amount of redundant spaces. One simple method of image steganography is the replacement of the least significant bit (LSB) of a cover image with a message bit. This represents a high embedding capacity but it is detectable by statistical analysis methods such as Regular-Singular (RS) and Chi-square analyses. Therefore, a new LSB algorithm is proposed here which can effectively resist statistical analysis. In this novel algorithm, every two sample’s LSB bits are combined using addition modulo 2 which is compared to the secret message. If these two values are not equal, their difference is added to the second sample. Otherwise, no change is made. This paper proposes a hardware realization of this new algorithm. Furthermore, two scalable pixel interleaver and novel message bit randomizer with two different stego-keys are designed. Pixel interleaver can improve resistance against visual analysis by random selection of pixels.
Hardware Architecture for a Message Hiding Algorithm with Novel Randomizers

- M. Bhat, G., Mustafa, M., A. Parah, S., Ahmad, J., 2010, ”Field programmable gate array
Hardware Architecture for a Message Hiding Algorithm with Novel Randomizers


Index Terms

Computer Science
Information Security

Keywords

LSB steganography; hardware description language; FPGA; pseudo-random number generator