Abstract

Operational transconductance amplifier (OTA) is one of the most significant building-blocks in integrated discrete-time filters used in analog to digital converter (ADC) for Sigma-delta converter. In this paper we designed a novel design method of two-stage CMOS amplifier in AMS 0.35\textmu m technology. P-Spice simulation results confirm the proposed OTA circuit. In fact, we achieved a gain band width (GBW) equal to 55 MHz, Cut-off frequency of 85 KHz and 57 dB gain (Av). In addition our new method allowed us to reduce settling time (St) to 15.6 ns and a slew rate (SR) of 0.1 V/\mu s at \pm 1.5V supply voltage. Eventually we have also succeeded in reducing the average power consumption to 1.65 mW while driving 3 pF load capacitor.

References

A Novel Design Method of Two-Stage CMOS Operational Transconductance Amplifier used for Wireless Sensor Receiver


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