Abstract

Multipliers and adders are the most significant part of all data path circuits in the microprocessor and digital signal processor. The power and speed of the multiplier and adder affects the entire performance of the system. In this paper, low power multiplier using Hybrid adder is proposed. Also it presents the analysis of three modified multipliers: Braun array multiplier, Baugh Wooley array multiplier, and CSA Multiplier with optimized adders. The multipliers are designed with optimized Hybrid and other adders using transistor sizing technique. The performance of power and delay of the multipliers are analyzed with optimization. All circuits are implemented in HSPICE BSIM model at 90nm deep submicron technology.

References

- Pedram, 1996, Power Minimization in IC Design, ACM Transactions on Design
Index Terms

Computer Science Integrated Circuits
Keywords
Dynamic Power  Cmosfa  Lpfa  Tgfa  Tgcdfa  Sfa  Cpl