Abstract

Floating point addition is more difficult than multiplication because alignment of mantissa is required before mantissa addition. The main objective of implementation of floating point adder on reconfigurable hardware i.e. on Virtex is to utilize less chip area with less combinational delay and faster speed. Less combinational delay means less latency i.e. less time is required to appear an output after the input response is applied and if there is less latency then there will be the faster speed and lesser the clock period. Implementation of floating point adder on Virtex 4 produces a least combinational delay of 24.201nsec consuming 4% of chip area while implementing same on Spartan 2 produces the greatest combinational delay of 79.594nsec consuming 92% of chip area. Less chip area means less number of slices is used in reconfigurable hardware i.e. on FPGAs.

References

- Alexandru, Mircea, Lucian and Oana, "Exploiting parallelism in double path adder
structure for increase throughput of floating point addition,” ©2007 IEEE.
- Metin Mete, Mustafa Gok, “A multiprecision floating point adder,” ©2011 IEEE.
- Florent de Dinechin, “Pipelined FPGA adders,” ©2010 IEEE.
- Ali malik, Soek bum ko, “Effective implementation of floating point adder using pipelined LOP in FPGAs,” ©2010 IEEE.
- Allan, Wayne Luk, “Parametised floating point arithmetic on FPGA,” ©2001 IEEE.
- Dr. John A. Eldon, Craig Robertson, “A floating point format for signal processing,” ©2002 IEEE.
- Asger, David, C. N. Iyu, “An IEEE complaint floating point adder that conforms with the pipelined packet forwarding paradigm,” ©2000 IEEE.

Index Terms

Computer Science

Algorithms

Keywords

Floating Point Addition  Fpgas  Vhdl  Xilinx