Field programmable gate arrays (FPGAs) are the reconfigurable logic devices which are widely used in many applications like system prototyping, complex computing systems, automotive electronics and mobile devices. FPGAs have become very popular at present because of their features like high logic capacity, reconfigurability and regular structure with less area cost. However, increase in density and complexity also has resulted in more probability of defects. FPGAs are prone to different types of faults similar to other complicated integrated circuit chips. Faults may occur due to many reasons like environmental conditions or aging of the device. The rate of occurrence of permanent faults can be quite high in emerging technologies, and hence there is a need for periodic testing of such FPGAs. To effectively deal with the increased defect density, we need efficient methods for fault detection and correction. Here, we present an approach for testing FPGA interconnect that exploits the reprogramability of an FPGA to create built-in self test (BIST) logic by configuring it only during off-line testing. In this way, testability is achieved without any area overhead, since the BIST logic "disappears" when the circuit is reconfigured for its normal system operation. We have used XILINX ISE12.1 for simulation and synthesis.
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Index Terms

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