Abstract

Reversible logic has attracted significance attention in recent years, leading to different approaches such as synthesis, optimization, simulation and verification. In this paper, we propose the design and optimization of n-bit reversible binary comparator. The circuit for MSB and one-bit comparator cell using NOT, PG and CNOT gates are designed. The n-bit reversible binary comparator is designed using circuit for MSB as first stage to compare MSBs and one-bit comparator cell as second stage and so on to compare lesser significant bit positions. The power consumption, delay, garbage outputs and constant inputs are computed. It is observed that the quantum cost and garbage output values are less in the proposed technique compared to the existing approaches.
Design and Optimization of n-bit Reversible Binary Comparator

References


Index Terms

Computer Science
Digital Circuits

Keywords
Reversible Binary Comparator  Quantum Cost  Reversible Logic  Garbage Output  Constant Input.